Large-Signal Design and Performance of a Digital PWM Amplifier[1]

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Large-signal performance of digital audio amplifiers is a critical parameter. Methods are described that improve the large-signal performance of a digital PWM modulator and feedback loop significantly. The resulting system is capable of maintaining excellent performance as the signal amplitude approaches the theoretical maximum duty ratio of 100%. The large-signal performance of a high-power digital PWM audio amplifier utilizing these methods is characterized in detail.

0 INTRODUCTION

Switching audio amplifiers can be broadly classified into two categories based on their pulse modulation method: 1) pulse-width modulation (PWM), and 2) pulse-density modulation (PDM). PWM-based amplifiers generally have a fixed switching frequency that is independent of the audio content. They also have a relatively lower switching frequency. PDM-based amplifiers have a higher average switching frequency, lower power conversion efficiency, and limitations in large-signal behavior [1]–[3].

PWM-based class-D digital audio amplifiers are becoming mainstream. Large-signal behavior is a critical parameter for audio amplifiers. The last few dB of volume represent most of the output power range of the amplifier. Meeting performance specifications at large-signal levels is critical. If the performance of the digital PWM amplifier at the limits of its duty ratio is not optimized then the amplifier has to be considered a lower power amplifier or the power supply rails have to be raised. Raising the power supply rail voltage or adding a boost switcher adds significantly to the system cost and reduces power conversion efficiency.

Digital PWM switching audio amplifiers form a class of high-efficiency class-D amplifiers in which a digital PWM signal is generated in the digital domain directly from a digital audio input. The digital PWM signal is amplified by either a half-bridge or a full-bridge switching power stage to drive an audio speaker. Typical digital audio sources include CD, DVD, SACD, and MP3 audio data. This approach has the benefit of maintaining the audio path in the digital domain from the input source to the switching power stage output.

The audio input for a digital PWM audio amplifier is usually in digital pulse code modulation (PCM) format. Conversion of PCM to PWM can be implemented in the digital domain with high resolution and accuracy [4]–[8]. Synchronization between the input PCM sample rate and the output PWM pulse repetition rate can be implemented using an asynchronous sample rate converter (ASRC) [9].

PWM pulse repetition frequencies for switching audio amplifiers typically range between 300 and 400 kHz. Pulse edges of digital PWM amplifiers are quantized in time using a much higher frequency PWM quantization clock f_Q, which is typically in the 20–100-MHz frequency range. Even at this frequency the duty ratio is quantized to a relatively low resolution of 6–8 bit. However, high-resolution audio performance can be achieved by incorporating an oversampled noise-shaping loop into the digital modulator. The PWM pulse edge data rate is about 16 times higher (4 octaves) than the input audio sample rate. Noise shaping pushes the PWM quantization noise out of the audio band. Optimum noise shaping takes into account the nature of the PWM signal [10]–[11]. In-band digital-domain dynamic range in excess of 20 bit is readily achieved with this approach.

Even though it is possible to exceed 20 bit of accuracy in the digital PWM signal, power stage nonlinearity and supply noise dramatically reduce the performance at the output of the power stage for an open-loop digital PWM system. To correct for these power-stage nonidealities an analog [12]–[13] or digital [14]–[16] feedback system is needed. Achieving power supply noise rejection and good large-signal behavior in a digital PWM amplifier requires feedback from the power stage. Implementation of a localized feedback loop around the power stage can be very effective. Such an amplifier is capable of delivering both excellent small signal as well as excellent large-signal performance. This topology requires that the large-signal behavior be optimized for both the digital PWM modulator block and the feedback loop circuit.

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1 SYSTEM OVERVIEW

Fig. 1 shows a general block diagram of the digital PWM audio amplifier system with localized feedback. The digital audio input is typically PCM at a sample rate of between 32 and 192 kHz. The upsampling block and optional asynchronous sample-rate converter (ASCR) provides an oversampled digital audio signal at twice the PWM pulse repetition rate, typically between 600 and 800 kHz. The PCM-to-PWM converter block incorporates predistortion signal processing designed to produce a highly linear PWM output signal from the PCM input. The noise shaper block implements the PWM edge quantization and shapes the subsequent quantization noise out of the audio band. The resulting PWM output signal is then used to drive a switching power stage.

Nonidealities associated with the power stage ultimately limit the overall performance of open-loop systems. The localized feedback loop is used to linearize the power stage and provide power supply rejection.

Both the PWM noise shaper and the feedback circuit are sensitive to large signals. Section 2 describes the large-signal operation of the digital PWM noise shaper. Section 3 describes the large-signal operation of the localized feedback circuit.

2 LARGE-SIGNAL OPERATION OF THE DIGITAL PWM MODULATOR

The noise-shaping portion of the digital PWM system consists of a sigma–delta modulator with a multibit quantizer and a high-order noise-shaping loop. Higher order noise shaping is used in order to achieve a high signal-to-noise ratio (SNR) and large dynamic range (DR) in the audio band. In our system we use third- and fourth-order noise-shaping filters. A specialized integral noise-shaping (INS) topology [10] is implemented that takes into account the PWM nature of the signal. The noise-shaping action results in a dither band that spans partially above and partially below the nominal desired output level. The PWM duty ratio cannot fall outside the range of 0–1. With large signals, as the nominal PWM output duty ratio approaches the limits of 0 or 1, the dither band will first begin to clip, followed by the nominal PWM signal itself (see Fig. 2). This will cause the system to saturate due to the accumulation of quantization errors. During this condition the accumulated errors will grow in an unbounded manner. When the saturation event goes away the system can go unstable or have an undesirable large-signal transient before resuming normal operation.

First-order feedback loops can go through a saturation event without going unstable or having undesired transients after the saturation condition goes away. Therefore it is desirable to reduce the system to a first-order loop during the saturation condition. It is also desirable to transition from a higher order loop to a first-order loop in a smooth fashion. To obtain the highest throughput in a digital signal-processing block it is desirable to implement these transitions without any conditional or branching operations.

Fig. 3 shows a block diagram of the basic PWM quantizer and INS noise-shaper system. This system is susceptible to instability when processing excessively large signals. Large-signal instability can be eliminated with the addition of the saturation handling features. The system shown is a third-order system with three stages of integration. The error between the unquantized and quantized PWM signals is integrated analytically as a computation in the digital domain. The introduction of the saturation handling feature is implemented by multiplication of a saturation function SAT with the integrands for the second and third integrals.

2.1 DIGITAL SATURATION FUNCTION

The saturation function SAT is used to adjust the gains of the noise-shaper feedback equations. It is desirable that the SAT function equal unity during small-signal operation (duty ratios centered about 0.5) and smoothly transition to a value of zero at the saturation duty ratios of 0 and 1. During small-signal operation the system is essentially unchanged. During large-signal operation the gains of the higher order integrators are reduced.

The saturation function can be defined using a piecewise-continuous function which is set to unity for the middle of the duty ratio range and obeys an appropriate polynomial function for the large-signal conditions. Fig. 4 shows three example saturation functions: SAT1, SAT2, and SAT3. Each of these functions has a different duty ratio range over which it is equal to unity. The range for SAT1 is 0.25–0.75; the range for SAT2 is 0.125–0.875; and the range for SAT3 is 0.0625–0.9375. The variable portions of these SAT functions are defined by the polynomials given in Tables 1–3.

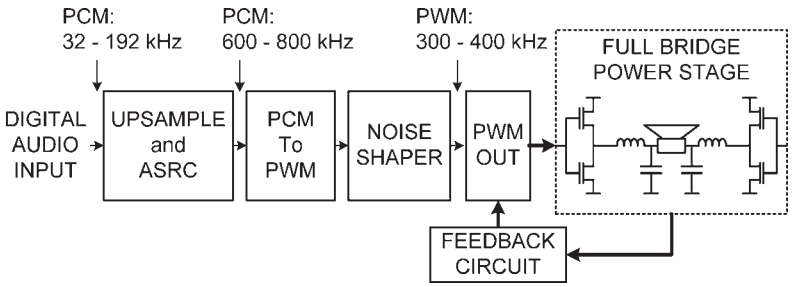

Fig. 1. Digital PWM switching audio amplifier system with local feedback loop.

2.2 POLE PLACEMENT

The INS system is implemented entirely in the digital domain. Consequently it is possible to design its system poles aggressively for performance. In contrast to an analog feedback loop that has to be robust to variations in component values, these pole locations are a function of the switching frequency, which is controlled by a high-accuracy clock signal. Each of the integrators contributes a pole to the system. PWM signals have two edges per pulse repetition period. The INS integrals are computed at some point in time after one PWM edge has passed and before the next PWM edge is to be produced. This delay between the computation and the subsequent edge contributes another pole to the system. Therefore a fourth-order INS loop with four integrals can be modeled with five poles. Similarly a third-order INS loop with three integrals can be modeled with four poles.

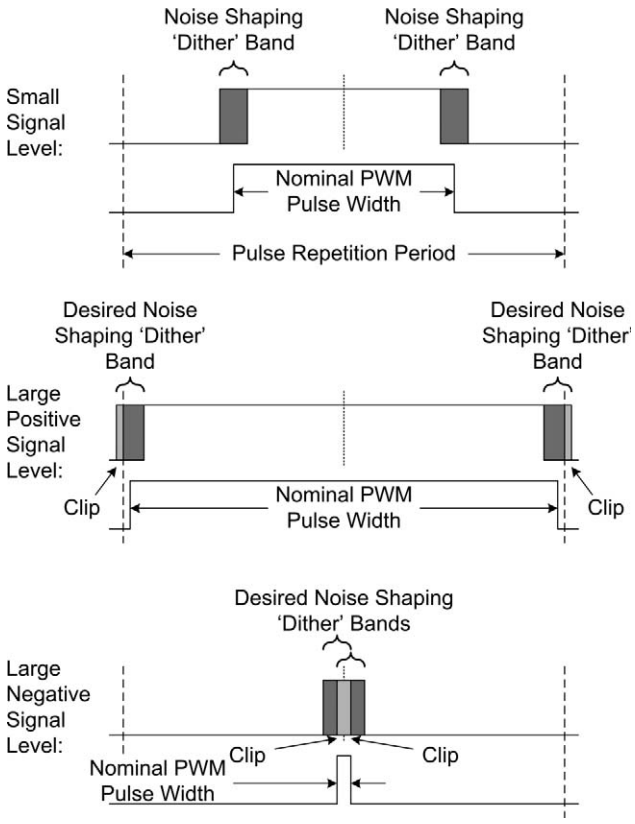

Fig. 2. Clipping of quantized and noise-shaped digital PWM signals.

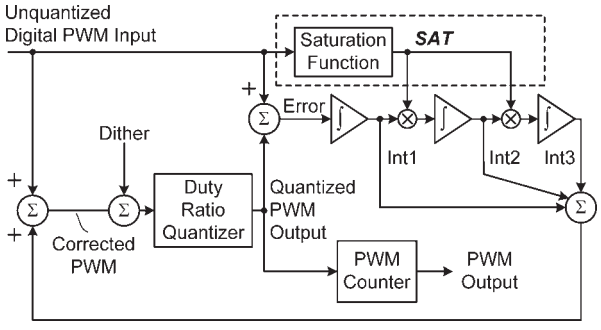

Fig. 3. System block diagram of third-order INS system with saturation handling.

In Fig. 5 the locus of the poles of a third-order INS modulator are shown. The system is modeled with four poles under normal operation. Locations of the poles are plotted as the value of the saturation function SAT changes from 1 to 0. The poles for SAT = 1 are indicated by circles; the poles for SAT = 0 are indicated by squares. For all values of SAT between 0 and 1 the pole locations are suitable for good stability. As a result the system operates well before, during, and after a saturation event.

Fig. 6(a) shows a simulated time-domain plot of the three integrals of a third-order INS modulator while processing a clipped 1-kHz sine wave. Two cycles of the sine wave processing are shown. The portions of the

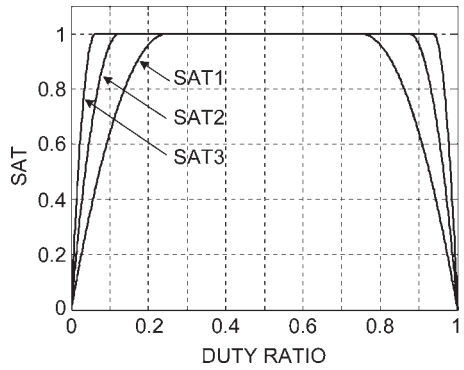

Fig. 4. Saturation function versus PWM duty ratio.

Table 1. Example SAT1 function.

Range of Duty Ratio, x	SAT1 Function
$0.0 <= x < 0.25$	$SAT = 8(x - 2x^2)$
$0.25 <= x <= 0.75$	$SAT = 1.0$
$0.75 < x <= 1.0$	$SAT = 8(3x - 2x^2 - 1)$

Table 2. Example SAT2 function.

Range of Duty Ratio, x	SAT2 Function
$0.0 <= x < 0.125$	$SAT = 16(x - 4x^2)$
$0.125 <= x <= 0.875$	$SAT = 1.0$
$0.875 < x <= 1.0$	$SAT = 16(7x - 4x^2 - 3)$

Table 3. Example SAT3 function.

Range of Duty Ratio, x	SAT3 Function
$0.0 <= x < 0.0625$	$SAT = 32(x - 8x^2)$
$0.0625 <= x <= 0.9375$	$SAT = 1.0$
$0.9375 < x <= 1.0$	$SAT = 32(15x - 8x^2 - 7)$

integrals that are flat correspond to the clipped, or saturated, portions of the signal. During a saturation condition the integrating operations continue, but since the integrands are zero the integral values do not change. Consequently at the end of the saturating event there are no large errors from which to recover.

Fig. 6(b) shows the corresponding simulated output duty ratio. Note that there are no undesired transients or ringing as the duty ratio transitions into or out of saturation.

Without the SAT function the INS modulator has a limited input signal range over which its operation is stable, as is typical with sigma–delta modulators. This stable input range becomes smaller with higher order modulators. This is often addressed by attenuating the input signal to within a stable range, at the expense of reducing the overall dynamic range. Implementation of the SAT function, however, completely eliminates the need to scale the input signal to maintain stability. This allows a full input range of 0–1. Next we will examine the large-signal performance of the PWM feedback loop.

3 LARGE-SIGNAL OPERATION WITH PWM FEEDBACK

The digital PWM modulator described in Section 2 is capable of generating a very high-fidelity audio signal in the digital domain. A dynamic range greater than 120 dB coupled with a total harmonic distortion of less than −120 dB and intermodulation of less than −110 dB is typical. However, when this signal is amplified to drive an audio transducer (loudspeaker), the overall performance is limited by the nonidealities of the switching power stage. For example, the switching dead time (or break before make) that is used to avoid large shoot-through currents results in high-order harmonic distortion. Nonlinear on-resistance of the power transistors also produces output harmonic distortion. In addition, since the switching voltage signal at the output of a switching power stage is determined by the product of the PWM duty ratio and the power supply voltage, an open-loop class-D amplifier has virtually no power supply rejection. Good open-loop performance requires extra complexity and cost to be invested into the design of both the switching amplifier and its associated power supply.

The addition of a properly implemented localized feedback loop around the power stage can result in exceptional distortion and power-supply rejection performance while reducing the complexity and cost of the power stage and power supply. Most PWM feedback systems are based on analog PWM modulators. The feedback system used in this work was targeted for use with a digital PWM modulator. It consists of a localized feedback loop wrapped around the switching power stage [14]. Fig. 7 shows a block diagram of the overall feedback loop system and Fig. 8 is a simplified circuit diagram of the corresponding loop filter.

PWM feedback systems have a curious limitation, which is independent of the implementation of the feedback loop. The limitation is that the only control over the system is adjustment of the PWM edges. Every PWM period has a rising and a falling edge, and these can be either advanced or delayed based on the error between the desired and the actual PWM waveforms. Further, for digital audio amplifiers the portion of the error that maps to the audio band is important.

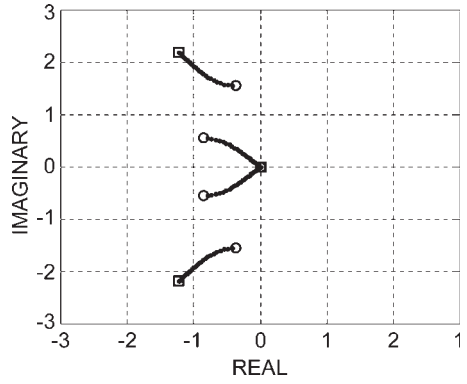

Fig. 5. Root locus of third-order INS modulator for SAT ranging from 1 (○) to 0 (□).

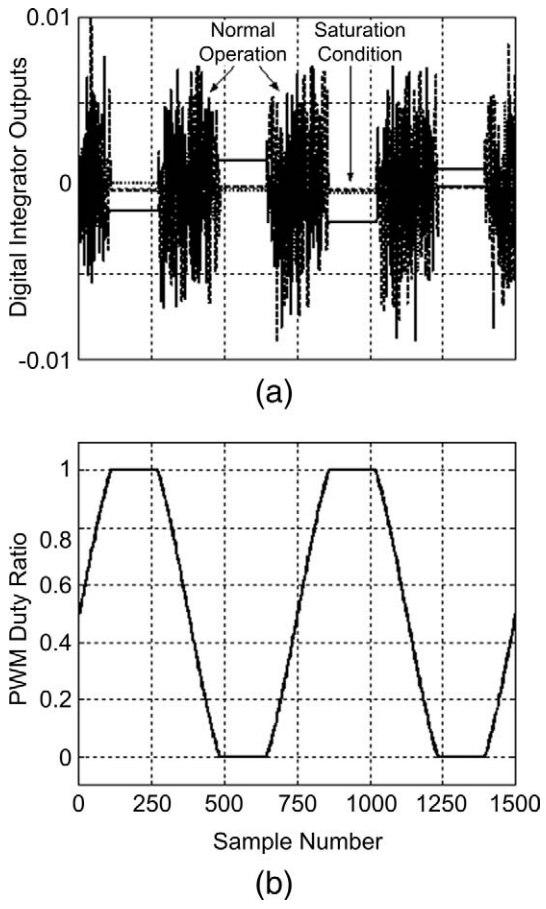

Fig. 6. Simulated integral outputs from a third-order INS modulator (a), corresponding to a clipped sine wave output (b).

In the feedback loop shown in Fig. 7 the loop filter consists of an integrating error amplifier (loop filter) that amplifies the difference between an ideal PWM reference signal and a scaled version of the actual PWM output waveforms. The output of the error amplifier is converted to digital using an analog-to-digital converter (ADC). The sample rate of the ADC is twice the PWM pulse repetition rate. In this way each ADC sample corresponds to a PWM edge, and each PWM edge is modified based on the corresponding ADC output sample. The corrected edge position is determined by summing the ADC output sample value with the position of the uncorrected edge. Fig. 9 shows the timing of the ADC sampling relative to the PWM edges being corrected.

A finite time delay, called the correction calculation latency, exists between each ADC sampling instance and the corresponding update to the digital PWM duty ratio counter. This delay includes the latency associated with the ADC and the time needed to update the PWM output counters. During large-signal conditions the depth of modulation grows, resulting in either very wide or very narrow pulse widths. Consequently the delay between the ADC sample point and its corresponding PWM edge can become very small. As this delay approaches the finite correction calculation latency the system can no longer provide the desired feedback correction. This puts a constraint on the maximum depth of modulation. As a result the large-signal performance of the feedback loop is limited.

This feedback system is compatible with both half-bridge and full-bridge power stage implementations. Half-bridge implementations have only one PWM signal with which to provide feedback control. However, a full-bridge power stage, as shown in Fig. 10, benefits from having twice the number of PWM control inputs (side A and side B). Two modulation modes are available with a full-bridge power stage. The first is standard PWM modulation, sometimes referred to as class AD modulation. The second is suppressed carrier PWM modulation, sometimes referred to as class BD modulation. Standard PWM modulation consists of a standard complementary pair of PWM signals in which the edge transitions on side B line up with the edge transitions on side A. Suppressed carrier modulation drives each side of the full bridge power stage with PWM signals that are substantially in phase with each other. With suppressed carrier modulation a large positive amplitude input signal produces a larger pulse width on the A side of the bridge and a smaller pulse width on the B side of the bridge. Similarly a large negative amplitude input signal produces a smaller pulse width on the A side of the bridge and a larger pulse width on the B side of the bridge. Suppressed carrier modulation produces a differential PWM output signal

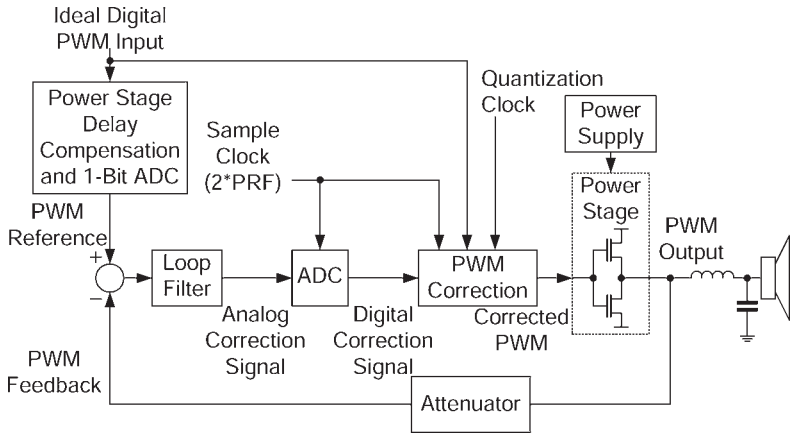

Fig. 7. Feedback loop block diagram.

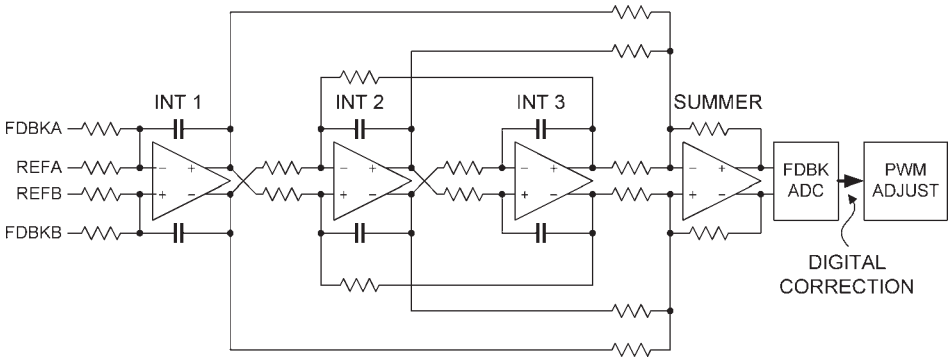

Fig. 8. Simplified circuit diagram of third-order feedback loop filter.

that results in the differential cancellation of the switching frequency and its odd harmonics.

Fig. 9 illustrates the feedback ADC timing using standard modulation with a full-bridge power stage. Each ADC sample provides correction to two PWM signal edges, one on the A side of the bridge and one on the B side of the bridge. Each corrected edge on the B side of the bridge continues to be time corrected with the corrected edge on the A side of the bridge.

For suppressed carrier PWM the edges on the two sides of the H bridge can be at different points in time. The duty ratios are set to be complementary such that the duty ratio on the B side of the bridge is 1 minus the duty ratio of the A side of the bridge. Fig. 11 shows the ADC sample points and the corresponding modified edges for suppressed carrier modulation.

Feedback loop gain is influenced by the number of PWM edges that are corrected per ADC sample. For example, the gain associated with the edge correction of the full-bridge system using either standard or suppressed carrier PWM modulation is twice that of the half-bridge system. This is due to each ADC sample providing correction to two PWM edges for the full-bridge case compared to each ADC sample providing correction to one PWM edge for the half-bridge case. To maintain good loop stability (for a given order loop filter) it is important that the loop gain remain steady. For a full-bridge system this requires that each ADC sample provide correction to two PWM edges. As stated before, extreme amplitude signals that push the PWM duty ratio toward either 0% or 100% create timing issues that result in undercorrected or noncorrected PWM edges. This creates two key problems. First the resultant degraded loop gain pushes the system toward instability. Second the increased errors in the corrected PWM output signal can lead to saturation in the loop.

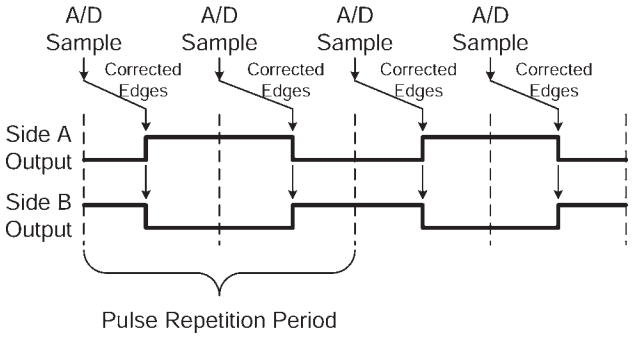

Fig. 9. ADC sample timing for standard PWM modulation.

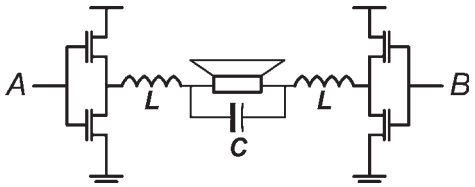

Fig. 10. Full-bridge class-D amplifier power stage.

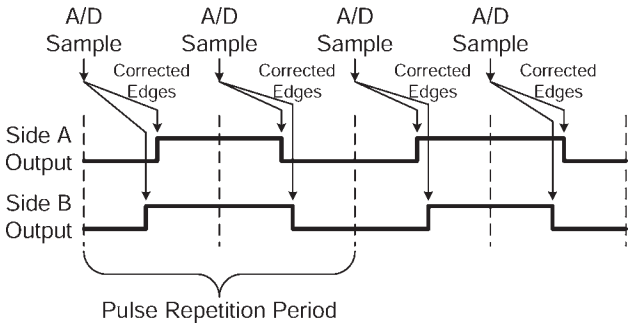

Fig. 11. ADC sample timing and PWM edges for suppressed-carrier PWM modulation during small-signal conditions.

3.1 VARIABLE-PHASE SAMPLING

Using suppressed carrier PWM modulation, the edge correction timing issues associated with large depth of modulation can be solved by dynamically adjusting the ADC sample time as a function of the PWM duty ratio. This is illustrated in Fig. 12(a) for the case of a small duty ratio signal and Fig. 12(b) for the case of a large duty ratio signal. For these extreme duty ratio cases the ADC sample timing has been shifted by a quarter of a PWM pulse repetition period. Maintaining proper loop gain requires that each ADC sample provide correction to two PWM edges. In these cases each ADC sample provides correction to the two subsequent PWM edges associated with either the side-A PWM signal or the side-B PWM signal. This approach mitigates the correction calculation latency issue, enabling the PWM duty ratio to be adjusted

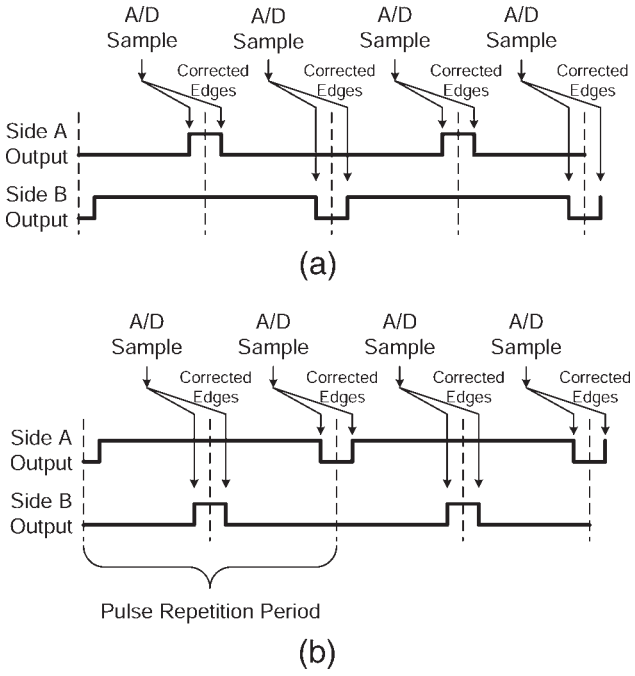

Fig. 12. ADC sample timing and PWM edges for suppressed carrier modulation. (a) Small duty ratio conditions. (b) Large duty ratio conditions.

all the way from 0 to 100% while maintaining stable operation.

Three modes of operation are defined. Mode A corresponds to small duty ratios, mode B corresponds to medium duty ratios, and mode C corresponds to large duty ratios. Typical audio levels result in duty ratios near 50% (mode B). For this case the ADC sample times are at the boundaries of each PWM half-cycle. As duty ratios increase or decrease beyond defined threshold levels the system transitions between modes B and C or between modes B and A. Each mode transition involves a quarter PWM cycle shift in ADC sample timing. Hysteresis is used to avoid transition chattering and to minimize the number of transitions. Fig. 13 diagrams the mode transitions, including hysteresis, as a function of duty ratio.

3.2 VARIABLE-LOOP ORDER

The feedback loop system can be viewed as a third-order noise-shaping modulator with a multibit quantizer (ADC). The error amplifier (loop filter) includes a cascade of three integrators. The error amplifier output is a weighted sum of the first, second, and third integrals of the error between the reference and output PWM signals. As with the digital INS modulator, the delay between the sampling of the error amplifier and the correction of the PWM signal results in an additional pole. Thus the system has four poles. The poles are placed on a unit circle to implement a fourth-order Butterworth design. Similar to the digital PWM modulator, saturation of the loop integrators can result in instability and poor performance.

The integrators and the ADC can saturate during large-signal transients. Instability due to these saturation events is mitigated by dynamically adapting the loop order as a function of saturation conditions. The output of each integrator is monitored. When saturation is detected the high order integrators are placed in an auto-zeroed reset state, effectively reducing the order of the loop. The system remains in the lower order state until the saturation condition is gone for a certain amount of hold time. This approach allows the system order to be reduced all the way down to a first-order system. A first-order system can go into and out of saturation without any undesirable ringing transient. Fig. 14 is a system-state machine diagram showing the system order transitions during saturation transients.

4 LARGE-SIGNAL SYSTEM PERFORMANCE MEASUREMENTS

The digital PWM generation lineup illustrated in Fig. 1 and the feedback circuit described in Section 3 have been integrated into an integrated circuit (IC). The IC receives audio input in the digital domain and produces a digital PWM signal with very high linearity and dynamic range. This digital PWM signal is output from the IC to drive an external power stage. Feedback signals from the external power stage are returned to the IC to correct for power-stage nonidealities. All of the following measurements were of the integrated PWM controller and feedback IC along with a discrete power stage. The programmable dead time for the power stage was set to 21 ns. This is the same hardware that was described and used in [14], which compared the closed-loop performance to the corresponding open-loop performance. The majority of the data were taken using suppressed-carrier PWM modulation.

4.1 ANALYSIS OF VARIABLE-PHASE SAMPLING

Closed-loop system performance using suppressed carrier PWM modulation with variable-phase ADC sampling was evaluated. Measurements were made using a power stage biased to 14.4 V and driving a 4-Ω load. The PWM switching frequency was 375 kHz and the PWM quantization clock frequency was 96 MHz, resulting in 128 quantization clocks per PWM half-cycle. The A-to-B and B-to-A thresholds are programmable in units of PWM quantization clock periods. The system implements the C-to-B and B-to-C thresholds based on the A-to-B and B-to-A settings to enforce symmetry.

The effectiveness of the variable-phase ADC sampling system for extending the large-signal performance of the amplifier is illustrated very clearly in Fig. 15. A family of measured THD+N curves versus output power for different ADC sampling phase transition thresholds is shown. The threshold hysteresis was fixed to 10 quantization clock periods while the B-to-A threshold value was varied. The case of A-to-B = 0 and B-to-A = 0 corresponds to the system operating only in mode B. For

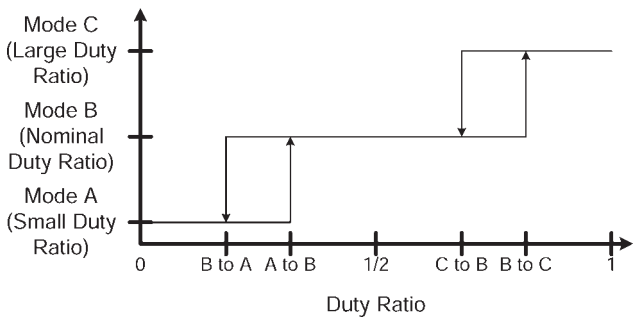

Fig. 13. Variable sample timing mode as a function of duty ratio.

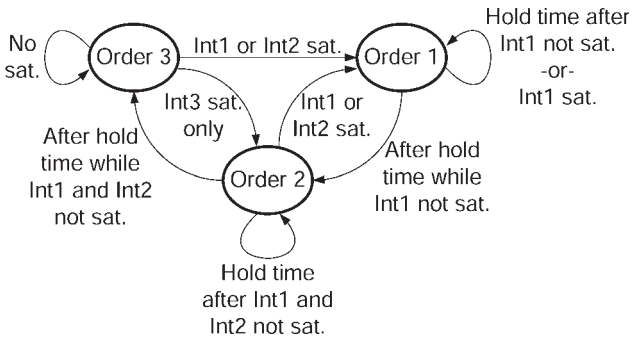

Fig. 14. State diagram for controlling order of feedback loop.

this case the performance begins a steep degradation as the signal power increases beyond ~12.5 W. This degradation is a result of the PWM duty ratio increasing beyond the timing constraints of the feedback loop correction system. This timing constraint includes the correction calculation latency coupled with the instantaneous digital correction value produced at the ADC output. Without sufficient head room to implement the required correction values large errors build up within the loop filter, resulting in rapid performance degradation. For the cases of the B-to-A transition threshold set to 10, 12, and 14 quantization clock cycles the system performance continues to begin to degrade at ~12.5 W, indicating that these B-to-A thresholds are too small. However, with these settings, as the signal power is increased the performance begins to improve until, ultimately, the signal level reaches hard clip. This region of improved performance occurs once the duty ratio value exceeds the B-to-A transition threshold and the system transitions from mode B to either mode A or mode C. The case of B-to-A set to 26 quantization clock cycles results in absolutely no performance degradation until the system begins to clip at beyond ~22 W. Thus with the appropriate mode transition thresholds, the variable-phase ADC sampling system increases the maximum undistorted output power by nearly 75%.

4.2 EFFECTS OF VARIABLE-ORDER FEEDBACK LOOP FILTER

As the corrected duty ratio signal reaches the hard limits of 0 and 100% the system begins to clip, as shown in Fig. 15, at an output power of about 22 W. Since a duty ratio beyond these limits cannot be realized, the error signal within the loop filter integrators increases to the point of saturation. As the loop filter saturation is detected the loop order is decreased from third order to first order according to the control state diagram in Fig. 14. The reduced-order loop filter maintains loop stability as the signal amplitude increases into hard clip.

Time-domain oscilloscope plots were captured for a 1-kHz sine wave output signal that is hard clipped at a 10% distortion level. Fig. 16 corresponds to the case where the order of the feedback loop filter is fixed to a third-order system and not allowed to vary. Glitches are observed in the waveform each time the signal transitions out of clip. This is indicative of momentary instability as the system tries to recover from its saturated integrator states.

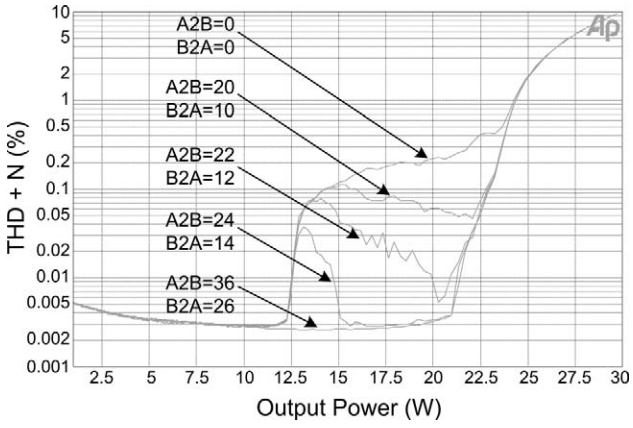

Fig. 15. THD+*N* versus output power as a function of B-to-A and A-to-B threshold settings.

Fig. 17 shows a corresponding time-domain plot for the case where the feedback loop filter is allowed to modify its order. Note that the ringing as the system transitions from full saturation to normal operation is entirely eliminated. The transition from full saturation to normal operation looks the same as the transition from normal operation to full saturation. In fact, the saturation transitions look very similar to that of a traditional class AB amplifier and close to the ideal saturation characteristics due to the limitation of the duty ratios at 0 and 100%.

4.3 MAXIMUM DEPTH OF MODULATION

The system described in this engineering report is capable of 100% modulation. However, many power stages that incorporate high-side NFETs rely on the PWM switching signal to drive a bootstrap circuit to generate a supply voltage greater than the power-stage supply for driving the high-side switch. These types of power stages cannot operate at 100% duty ratio and generally require or specify a minimum pulse width.

To accommodate a variety of external power stages that may require minimum output pulse widths, our system incorporates a programmable "guardband" that sets the PWM output clip level. A guardband setting of 0 allows the PWM duty ratio to clip at its theoretical maximum of 0 and 100%. Nonzero guardband settings are programmable in units of two PWM quantization clock periods, resulting in steps of 20.8 ns with a PWM quantization clock of 96 MHz. For this case a guardband setting of 1 will clip the output PWM signal to a minimum pulse width of 20.8 ns. Similarly a guardband setting of 7 will clip the output PWM signal to a minimum pulse width of 145.8 ns. Fig. 18 shows the THD+*N* performance as a function of output power for minimum PWM pulse widths ranging from 0 to 145.8 ns.

These figures illustrate the reduced dynamic range of undistorted peak power associated with limiting the peak depth of modulation. Power stages that do not require minimum PWM pulse widths for accommodating a bootstrapped gate drive supply clearly have a dynamic range advantage. The need for a bootstrapped supply can be eliminated by implementing a charge pump circuit, independent of the PWM signal, to generate the appropriate high-side gate drive supply voltage. This approach allows unlimited PWM depth of modulation and maximum undistorted output power for a given power-stage power supply voltage. Alternatively a power stage with a *p*-channel high-side FET can be driven to 100% depth of modulation without either a bootstrapped supply or a charge pump.

If a minimum PWM pulse width is unavoidable, the power-stage supply voltage can be increased to achieve desired peak output power. However, a higher rail voltage results in lower efficiency due to higher switching losses. Efficiency actually improves when clipping to 0 and 100% modulation, since no switching occurs during these times. For an optimized power stage that has equal switching and resistive losses, the losses are halved during 100% modulation. In order to achieve full 100% modulation both the digital PWM modulator and the power stage must have 100% modulation capability. Having 100% modulation capability puts the system's output power capability on par with class A/B amplifiers.

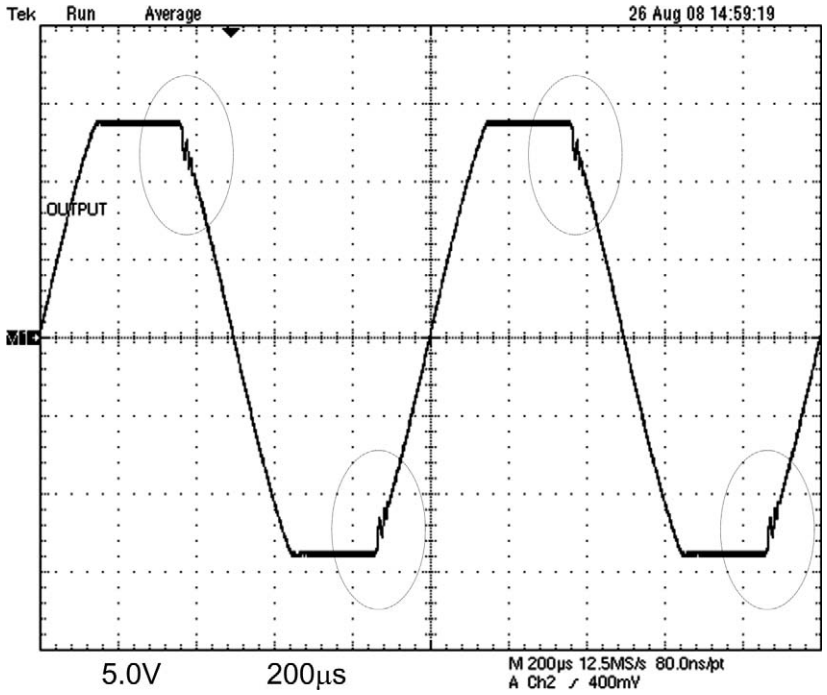

Fig. 16. Measured 1-kHz signal clipped at 10% distortion. Feedback loop order is fixed at third order. PWM duty ratio allowed to extend to 100%.

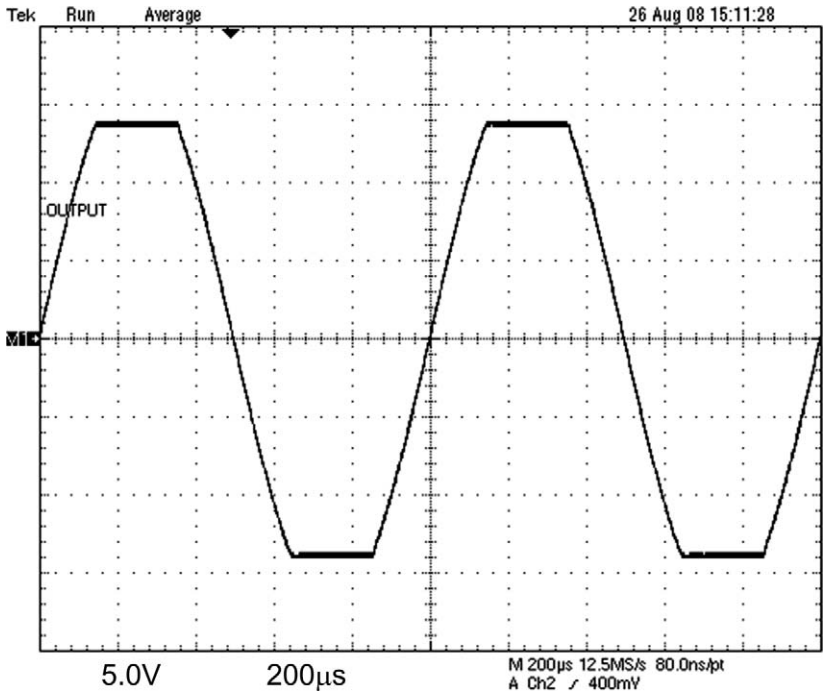

Fig. 17. Measured 1-kHz signal clipped at 10% distortion. Feedback loop order is allowed to vary between first and third order. PWM duty ratio allowed to extend to 100%.

4.4 PWM REFERENCE AND FEEDBACK DC AMPLITUDE MISMATCH

As previously noted and illustrated in Fig. 7, the feedback system operates on the error between the PWM feedback signal from the power stage and a PWM reference signal. This error results from both dynamic mismatch between the feedback signal and the reference signal (due to power stage nonidealities and power supply noise) and from nominal pulse amplitude mismatch between the feedback signal and the reference signal. Nominal pulse amplitude mismatch can degrade the large-signal performance of the amplifier.

The nominal pulse amplitude of the PWM reference signal is determined by a reference dc voltage. The nominal pulse amplitude of the PWM feedback signal is determined by a combination of the power stage supply voltage, the IR drop across the power FETs, and the feedback attenuation network. When the nominal pulse amplitude of the feedback signal is less than the nominal pulse amplitude of the reference signal the feedback correction will tend to increase the output PWM pulse width. When the nominal pulse amplitude of the feedback signal is greater than the nominal pulse amplitude of the reference signal the feedback correction will tend to decrease the output PWM pulse width. This is illustrated in Fig. 19 for the case of suppressed carrier PWM modulation.

Ultimately feedback correction is provided so that the total area of the output feedback PWM pulses is equalized to the total area of the PWM reference signal. Note that this is implemented differentially. Therefore when the duty ratio is at 50% the feedback correction is nominally zero, independent of any mismatch between the feedback signal dc amplitude and the PWM reference dc amplitude.

Fig. 20 shows the relative amplitude and polarity of the feedback correction as a function of the PWM reference duty ratio and relative nominal pulse amplitude of the feedback signal compared to the nominal pulse amplitude of the reference. A negative correction translates to reducing the duty ratio. A positive correction translates to increasing the duty ratio.

For the purposes of this study, the PWM reference amplitude was set to correspond to a nominal power supply voltage of ~14.4 V. Measurements of THD+N versus output power into 4 Ω for a 1-kHz tone were taken for power-stage power supply voltages ranging from 13 to 17 V. These data are shown in Fig. 21.

The bump in the THD+N curves located at about 7 W is associated with the B-to-A and A-to-B setting of the variable sample point system. For the given setting of B-to-A = 26 and A-to-B = 36, signal levels below 7 W are not large enough to transition out of mode B. Signal levels greater than 7 W are sufficiently large that they require transitions into and out of modes A and C. It is observed that the amplitude of this bump is a function of the power-stage power supply. For the case of $V_{dd} = 14$ V this bump is nearly nonexistent. For the case of $V_{dd} = 17$ V this bump is relatively large. There is a nonlinearity associated with the A-to-B/B-to-A transition. The larger the dc mismatch ?2

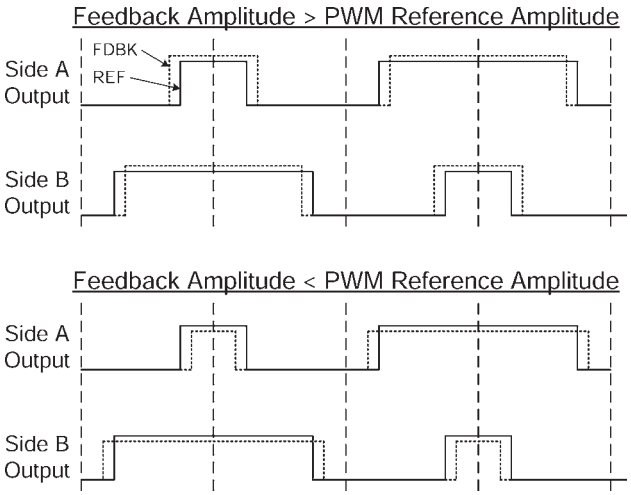

Fig. 19. Example of feedback correction with dc amplitude mismatch between feedback signal and reference PWM signal. —— = PWM reference, – – – = PWM feedback signal.

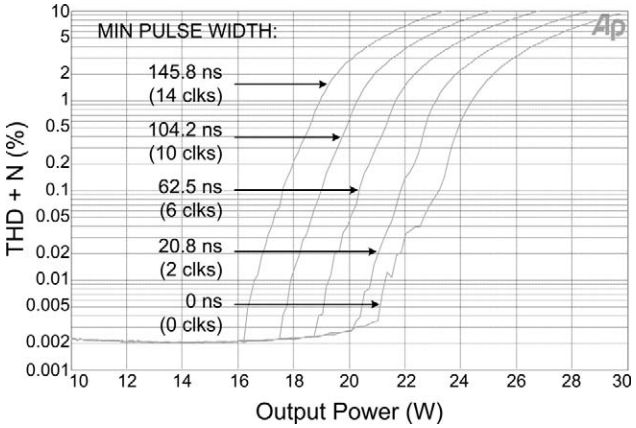

Fig. 18. THD+N ratio versus output power for different minimum pulse width settings. $V_{dd} = 14.4$ V; load = 4 Ω, 1 kHz. Minimum PWM pulse widths in units of 96-MHz clock periods.

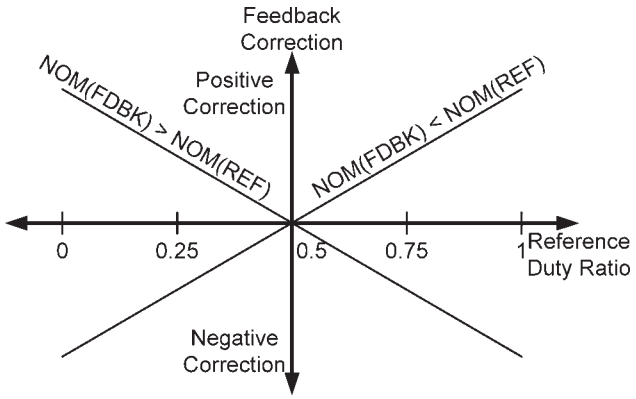

Fig. 20. Relative feedback correction versus reference duty ratio for NOM(FDBK) > NOM(REF) and NOM(FDBK) < NOM(REF).

between the feedback voltage level and the PWM reference level, the larger the nonlinearity. Changing the phase of the ADC sample point results in a change in the ADC output correction value. This correction change is scaled by the dc mismatch between the power-stage power supply amplitude and the PWM reference amplitude. For a given B-to-A setting the bump is positioned at the same power level independent of the supply voltage. This is due to the fact that the present design monitors the input reference duty ratio to determine when to transition between modes A, B, and C. Alternatively one could monitor the output (corrected) duty ratio.

Referring to the measured data in Fig. 21 at power levels lower than 7 W, better noise performance is observed with larger supply voltage. For a given power output the higher supply case requires a smaller range of output duty ratios. The smaller range of output duty ratios translates to better power-stage linearity. Since the power-stage nonlinearity mixes the out-of-band noise associated with the noise-shaped digital PWM modulator into the audio baseband, the improved power-stage linearity results in better noise performance. This helps demonstrate that even at lower power the effect of the power-stage nonlinearity dominates the noise floor.

4.5 SAT FUNCTION AND DITHER

It has been well established in theory that adding appropriate dither to the quantization process is beneficial [17]. Dither added prior to the quantizer acts to "whiten" the spectrum of the quantization error. This can prevent the generation of limit cycles and idle tones at low signal amplitudes. Dither having a triangular probability density function has been shown to have certain optimal characteristics. This type of dither has been incorporated into the digital INS PWM modulator, as shown in Fig. 3.

Addition of the dither signal increases the variation in the PWM duty ratio. This corresponds to an increase in the noise-shaping dither band illustrated in Fig. 2. The effect of the dither can be observed under certain large-signal conditions. However, its observability can be hidden by the large-signal saturation behavior of the feedback loop. This issue can be addressed by increasing the power-stage power supply voltage so that the dc amplitude of the feedback signal exceeds the dc amplitude of the PWM reference. This ensures that the corrected PWM signal never clips to 0 or 100% and the feedback loop filter never saturates. A power supply voltage of 17 V was chosen for these measurements, compared to a nominal supply of 14.4 V.

Under these conditions the THD+N ratio versus output power of the amplifier was measured both with and without dither. Fig. 22 shows that the bump in the nonlinearity related to the variable sample point transition occurs at a slightly higher power level (~8 W) with dither turned off, compared to ~7 W with dither turned on. The bump is also more abrupt with the dither turned off. The reason for this is that the dither increases the duty ratio excursion, and the B-to-A (B-to-C) variable sample point transitions are related to the value of the uncorrected duty ratios. When dither is turned off these transitions do not occur until the output power approaches 8 W. When dither is turned on these transitions start at about 6.5 W.

There is a more striking difference between the amplifier behavior with dither and without dither at power levels approaching clip. When dither is off, the linearity remains at a very high level (~90 dB) until the output signal clips at about 23 W. When dither is on, the linearity degrades to a level of about 70 dB for a small range of signal levels just below clip (~21–23 W). Beyond 23 W the linearity behavior is identical whether dither is on or off. This is clearly illustrated in Fig. 23, which shows a zoomed in view of the clip transition. At power levels above 23 W the duty ratio saturates at the peaks of the input sine wave corresponding to the clipped input signal. Dither is of no consequence under the saturation condition. However, the increased width of the PWM dither band when dither is enabled triggers duty ratio saturation at power levels just below actual signal clip (~21 W in this case). The degraded linearity in this region corresponds to signal levels that are below actual signal clip, yet are large enough to where the increased dither band begins to clip.

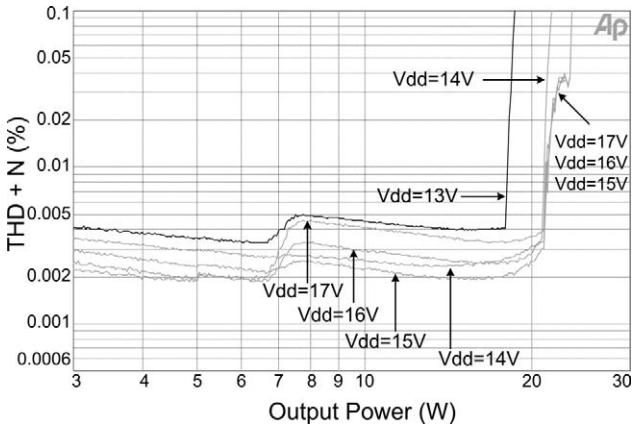

Fig. 21. THD+N versus output power for power-stage power supply voltages of 13, 14, 15, 16, and 17 V; load = 4 Ω; 1 kHz.

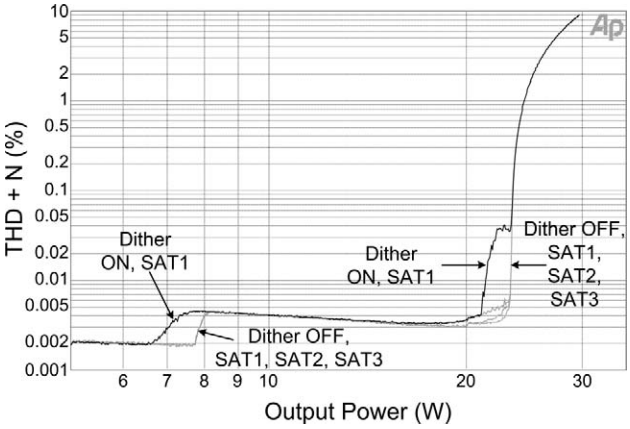

Fig. 22. THD+N versus output power showing effects of dither and SAT function. $V_{dd} = 17$ V; load = 4 Ω; 1 kHz.

The effect of the SAT function on large-signal performance of the amplifier can be readily observed when dither is turned off. This is shown in Fig. 23 for the three SAT functions (SAT1, SAT2, and SAT3) that were described in Section 2.1. Although the differences are relatively small, the SAT3 function provides the best large-signal performance, and the SAT1 function provides the worst. This can be explained by the plot of the SAT functions in Fig. 4, which shows that SAT1 begins attenuating at a smaller depth of modulation than the SAT3 function. When the saturation function becomes less than 1 the INS loop gain is reduced and overall noise and distortion are increased. The saturation function cannot be eliminated without causing stability problems. Note, however, that the large-signal performance differences between the different SAT functions are all but obscured when dither is enabled.

4.6 OVERALL SYSTEM PERFORMANCE

Fig. 24 shows a plot of THD+N ratio versus output power of a 1-kHz tone into a 4-Ω load for the overall system. Operating conditions include:

- Suppressed carrier modulation with a third-order digital INS noise-shaping filter
- SAT1 saturation function
- Dither enabled
- PWM quantization clock = 96 MHz
- PWM switching frequency = 375 kHz
- Variable sample point settings of B-to-A = 26, A-to-B = 36
- V_{dd} = 14.4 V
- PWM duty ratio clips at 0 and 100%.

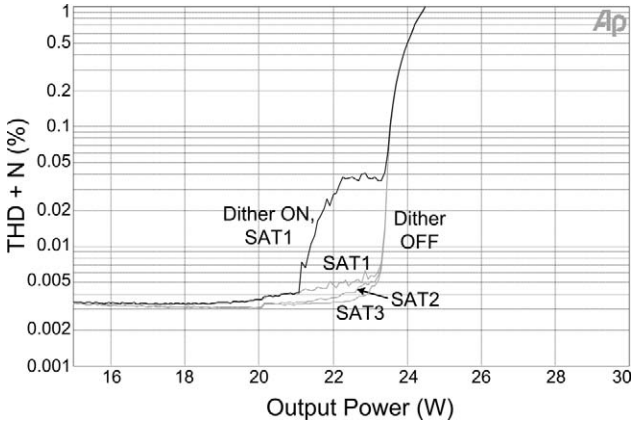

Fig. 23. Zoomed-in view of data in Fig. 22.

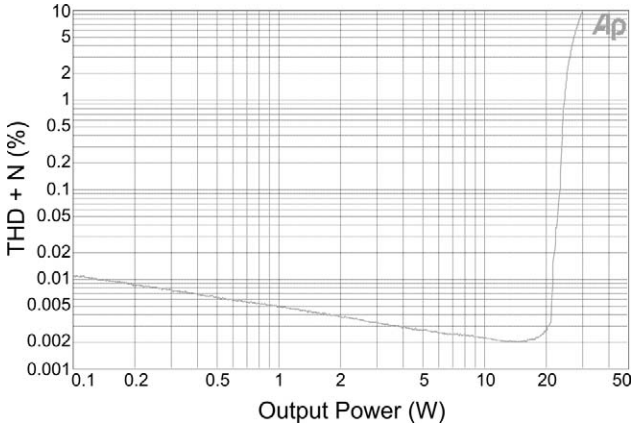

Fig. 24. THD+N versus output power for overall system. V_{dd} = 14.4 V; load = 4 Ω; 1 kHz.

The supply voltage of 14.4 V provides a feedback amplitude that is matched to the PWM reference level, resulting in a negligible bump at around 7 W. The THD+N ratio is mostly dominated by the noise floor for all signal levels up to the point of signal clip. The minimum THD+N ratio is 0.002% and occurs at just below 20 W. The 0.1% distortion level occurs at an output power of ~23 W. The 10% distortion level occurs at an output power of ~30 W.

5 CONCLUSIONS

This engineering report describes a digital amplifier system that demonstrates excellent large-signal properties. A number of system features have been combined to seamlessly transition from a higher order noise-shaping loop that exhibits ultra low-noise small-signal behavior to a first-order loop producing a theoretical maximum saturation duty ratio of 100%.

A high-fidelity feedback loop corrects power-stage nonidealities to provide very high linearity at large power levels. Techniques such as variable-order feedback and variable-phase sampling enable the system to squeeze out high accuracy at duty ratios approaching 0 and 1.

The overall system exhibits linearity that far exceeds 80 dB (or 0.01%) total harmonic distortion at power levels almost twice that of a similar closed-loop system without these techniques. This enables a reduction in power supply voltage rails with accompanying benefits of reduced losses, smaller power stages, and elimination of boost converters in automotive amplifiers.

In summary, this digital PWM amplifier system has much higher efficiency and linearity than comparable class AB amplifiers while having similar large-signal saturation characteristics. The large-signal behavior includes graceful saturation to duty ratios of 0 or 1, which approaches the theoretical best large-signal performance possible from a switching amplifier. Detailed measurements of the system at various amplitude points support this claim.

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