AN ALL-DIGITAL UNIVERSAL RF TRANSMITTER

Poojan Wagh, Pallab Midya, Pat Rakers, James Caldwell, and Tony Schooler

Motorola Laboratories
Schaumburg, IL, USA

Abstract

This paper presents a CMOS Class D PA with on-chip all-digital RF modulator. The IC is fabricated in a 0.18 um digital CMOS process with MIM capacitors. The die size is a square 2.5 mm on each side. The active area used for the modulator (excluding the pads and bypass capacitance) is 0.315 mm^2. The class D PA shows 75 dB IM, -50 dB feed-through, and puts out 19.6 dBm at >69% drain efficiency from a 1.8 V supply. The modulator operates in the IQ domain, without the use of bias control nor envelope modulation.

Introduction

Conventional linear power amplifiers (PA's) are generally inefficient at producing power. This causes increased current drain in wireless hand-helds, reducing talk- and standby time. Switched-mode PA's are more efficient, but they are not linear and therefore cannot support signals with moderate or high peak-to-average ratios (1).

Methods which encode the desired modulation within a switching waveform offer the best of both worlds. The switching waveform is composed of the desired modulation plus out-of-band noise or harmonics, which can be filtered away. In addition, since the modulator now produces a 1-bit signal (the switching waveform), the modulator itself can be made out of digital building blocks (2).

We intended to design and build a class D CMOS PA and associated modulator which could demonstrate the linearity, power efficiency, and reduced complexity of such an all-digital system.

The paper is organized as follows: the first section explains the signal scheme used in the modulator. The second section describes the test IC in detail. The third section describes how the measurements were taken. The fourth section presents the measured results.

Quadrature Pulse Modulation

The method we propose to encode the signals has been termed Quadrature Integral Noise Shaping and is discussed in detail in (3). A brief explanation is provided here for clarity.

This method is more aptly named Quadrature Pulse Modulation (QuadPM), in that the technique can be used for any type of pulse modulation, including pulse width modulation (QuadPWM) and pulse density modulation (QuadPDM).

As shown in Figure 1, QuadPM operates by taking two 1-bit signals pm_I and pm_Q (representing in-phase (I) and quadrature (Q) signals, respectively) valued ±1. The signals may be produced by PWM, PDM, or any other method which can linearly encode the desired I and Q modulation into 1-bit form. Mathematically, two local oscillator (LO) signals LO_I and LO_Q are used to modulate these 1-bit signals to produce the output y:

$$y[n] = pm_I[n] * LO_I[n] + pm_Q[n] * LO_Q[n] \quad (1)$$

Since LO_I is only non-zero when LO_Q is zero (and vice versa), y is a 1-bit output. In addition, pm_I is synchronized to LO_I and pm_Q is synchronized to LO_Q before modulation. This means that the multiplication does not inject any additional transitions in the output.

Although mathematically, the LO's and PWM signals are represented as 3-level values, all the intermediate signals and the final output can be performed with digital logic (essentially a set of multiplexers).

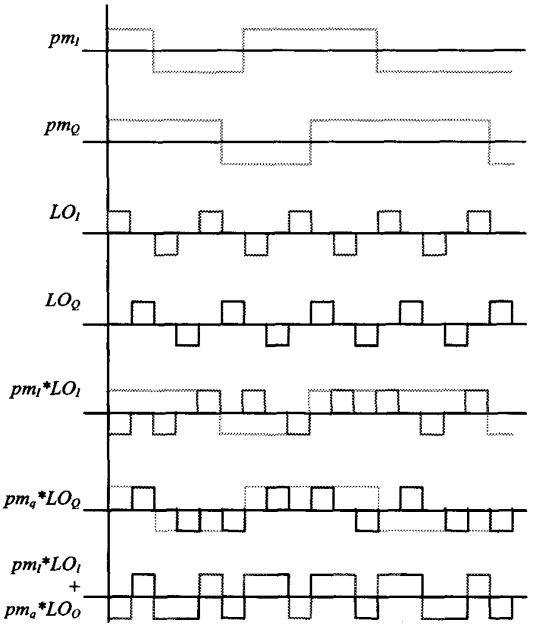

Figure 1: Timing Diagram for Quadrature PWM

The advantage of this approach is that the noise shaping loop can run at a lower rate than the modulator and therefore at a lower rate than the desired RF carrier frequency. In addition, the smallest pulse width, a quarter of the carrier period, occurs rather infrequently. Usually, the pulse width is half

the period which is the same as it would be for a continuous wave carrier. A band-pass sigma-delta running at 4x the carrier frequency would frequently produce pulses with widths of a quarter of the carrier period. These small pulse widths could affect the linearity of the power stage.

The disadvantage of this approach is that if QuadPWM is used, the RF output will include large switching harmonics which will then need to be suppressed by a filter. If QuadPDM is used, then one gives up some resolution since the noise-shaping loop will be running at a rate lower than the RF carrier frequency. (One could choose to run each PDM noise-shaping loop at the maximum rate of twice the RF frequency. However, in that case, the system has little advantage over a band-pass delta-sigma running at 4x the carrier frequency as described in (2).)

The Test IC

The test IC was fabricated in order to measure the linearity of a CMOS class D PA (a CMOS inverter). At the time of design, QuadPWM was the most promising technique. Since it would be difficult to drive the signals onto an IC containing the PA, the QuadPWM modulator was built together with this PA.

Figure 2 shows a block diagram of the test IC. A clock reference at f_{Master} (4x the carrier frequency) is sent onto the IC. This master clock is squared up and then provides timing for all the digital logic which generates the PWM and for the modulator itself.

The digital PWM generator accepts duty ratio values. These values are pre-distorted (4) and noise-shaped (5). The duty ratios are 6-bit values, representing 64 possibilities per PWM edge.

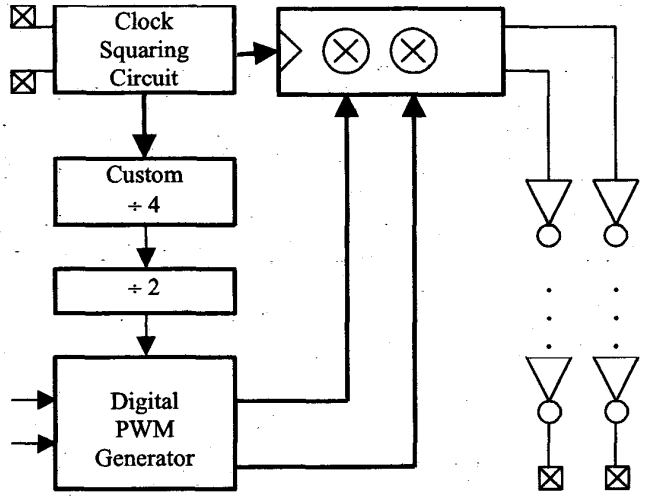

Figure 2: Block diagram of test IC

A variable divide ratio from the master clock sets the transition clock for the PWM (the quantization clock) to $f_{Master}/16$. The switching frequency is programmable from a minimum of $f_{Master}/1024$. Since f_{Master} is 2.6 GHz, the minimum switching frequency is 2.53 MHz. In addition, since the quantization clock is fixed $f_{Master}/16$, the maximum resolution is 64 levels. Increasing the switching frequency allows for more bandwidth, but increases the quantization noise. Although this IC was designed with the quantization clock fixed at $f_{Master}/16$, it could have been set at $f_{Master}/2$; one can get more resolution out of the QuadPM system than is demonstrated with this IC. Unfortunately, the digital logic could not run at this high rate.

The 1-bit signal from the modulator goes through several stages of build-up, formed by CMOS inverters, and then drives the final PA. The widths of the final PA were sized by simulation to provide the highest efficiency. If they are sized too large, switching losses will dominate. If they are sized too small, resistive losses will dominate.

The supplies of the output stages were limited to 1.8 V. Off-chip matching networks were intended to transform a 50-Ohm load down to 8 Ohms so that 65 mW of output power could be generated.

As shown in Figure 3, the output stage has a separate power supply. This allows for the measurement of current going through the output stage, from which we can compute the drain efficiency (DE).

The series resonant LC circuit at the output of the power stage rejects high-order harmonics, allowing for a sinusoidal output current and a square drain waveform. Since the output current is sinusoidal, no power is actually created at the harmonics (assuming a high enough Q for the loaded LC). Since the output voltage is a rail-to-rail square wave, this output stage has less variation and requires less power control than typical linear PA's.

In this design, the output bond-wire yields the inductance. An off-chip DC blocking capacitor is used in conjunction with a double-slug tuner to produce the capacitive impedance.

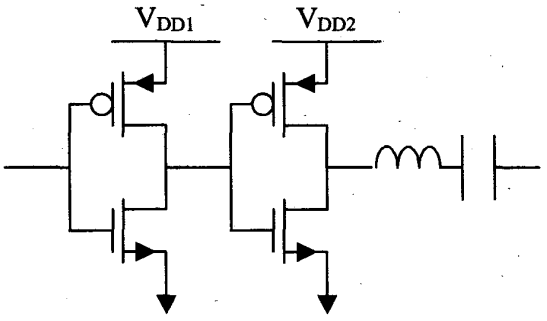

Figure 3: Schematic of Driver and Output Stage

Figure 4 shows a block diagram of the modulator core. As stated before, the modulator core is essentially a set of digital multiplexers. The master clock drives each flip-flop. The final flip-flop in the modulator determines the phase noise of this system.

The RF circuitry was custom-designed digital logic. Where

possible, circular FET layouts were used to reduce diffusion capacitance.

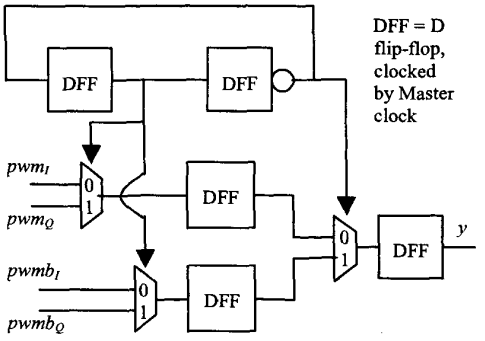

Figure 4: Block Diagram of Modulator Core

Figure 5 shows the layout of the IC. In the center is the core modulator. To the left of the modulator are the clock squaring circuits, and to the right is the synthesized digital logic. The driver stages are to the lower left, and the two output stages are built into the corner pads in the lower left.

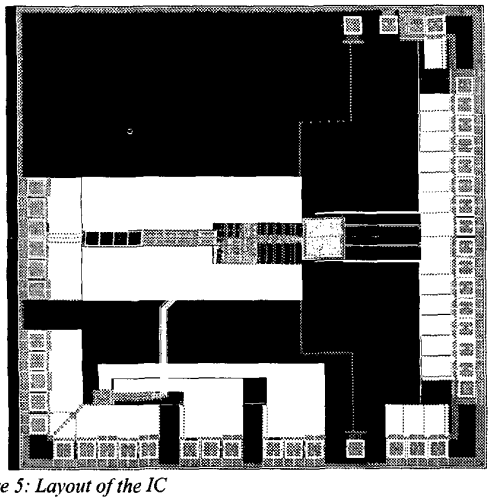

Figure 5: Layout of the IC

Measurement Setup and Calibration

The IC was mounted on an FR-4 substrate. The output transmission lines were designed to be 50-Ohm coplanar wave-guide (CPW).

In order to measure the linearity of the output devices, a low impedance needs to be presented to the IC. Since there is a CPW transmission line on the board, one cannot directly measure the impedance presented to the IC.

Instead, a double-slug tuner was placed after the board. A double-slug tuner is a set of two dielectrics ("slugs") embedded within a coaxial air line. By varying the positions of the slugs, the impedance presented to the board can be varied. By varying the impedance, one can maximize output power. One can reasonably assume that at the peak output power, the lowest possible impedance is being presented to the IC, even though one cannot directly measure it.

A spectrum analyzer (SA) was used to measure the output power in this case. This can add measurement uncertainty. To offer some calibration of the SA measurement, a signal source was connected to the SA and the difference between the signal source power and the SA measurement was recorded and was used to correct the SA measurements. The loss in the double-slug tuner was measured by taking 2-port S-parameter measurements.

In order to drive the modulator with data, a pattern generator was used. The pattern was a sequence of PWM duty ratios, consisting of a desired signal and shaped noise. The pattern generator was set up to repeat the sequence continuously. The shaped noise is repeated by default. The signal period was chosen (where possible) to be a multiple of the pattern period. The pattern repeated every 15 ms, so the tone frequency for the two-tone test was chosen to be a multiple of 66.7 Hz.

An Enhanced Data Rate for GSM Evolution (EDGE) test was done. EDGE is an offset 8-level phase-shift keyed modulation (8PSK). The EDGE data was produced by taking a pseudo-random bit stream (PRBS), producing offset 8-PSK, and running it through the prescribed symbol shaping filters to produce IQ data. Enough start-up bits were added to the beginning of the PRBS to ensure that the filtered IQ data repeats as desired.

Since noise shaping is involved, some signal headroom had to be allocated below full-scale to keep the noise-shaping loop stable. In this case, we chose -12 dB_{FS} as the maximum. If greater timing resolution were available, a larger signal could be generated since less headroom would be needed for noise shaping. The noise shaping loop chosen for these measurements was a 4^{th} order integrator with 2 non-dc noise-transfer zeros.

For the 2-tone test, a 2.53 MHz switching frequency was chosen to allow the lowest quantization noise. For the EDGE tests, a 5.06 MHz switching frequency was chosen to allow for larger bandwidth.

For all measurements, 100x video averaging was used to smooth out the noise spectra. The resolution bandwidth and video bandwidth were both set to be 0.2% of the frequency span.

Measurements

When reset is active on the IC, the PWM does not switch. Consequently, the IC outputs a simple square wave at the RF frequency. In this manner, one can effectively test the full-scale power capability of the output stage. With the optimized double-slug load, the full-scale output is 19.46 dBm. At this output power, the output stage draws 71.1 mA of current from the 1.8 V supply. The simple drain efficiency is 69.0 %.

The drivers between the modulator and the output stage draw 34.6 mA. The modulator core, clock squaring circuits, and digital logic draw 61.6 mA, the majority of which is drawn by the clock squaring circuits. The clock squaring circuits were over-designed to ensure fast edge rates and to reduce risk.

In addition, the currents given above are for two sides of the differential circuit. However, since a balun was not available, the output powers given above are only for a single side of the differential output stage. With a fully differential output, twice the voltage (and therefore 4x the power) could be generated. Since the inactive side is terminated in a relatively high impedance (50 Ohms), the current listed above will not be much higher than the current for the active side.

Figure 6 shows the results of the 2-Tone test. The worst-case harmonic is the fifth, which is –75 dBc. In addition, there is a feed-through term of –53 dBc.

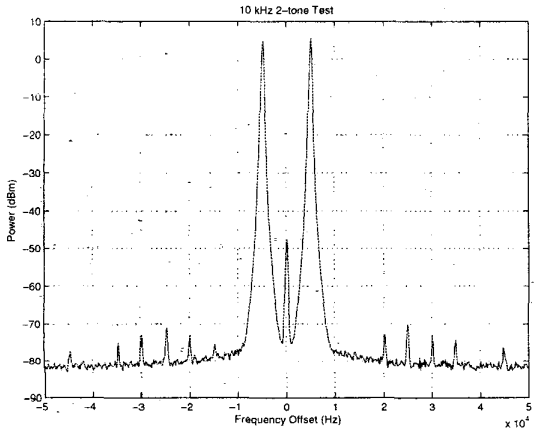

Figure 6: In-band 2-Tone Spectrum

Figure 7 shows the wideband spectrum around the 2-tone. Due to the large frequency span, it appears as a single tone. One can see the shaped noise. Approximately 1 MHz of clean (noise-suppressed) bandwidth is preserved.

Figure 8 shows an ideal EDGE input, an EDGE ACPR Mask, and the EDGE spectrum at the output of the IC. From a linearity perspective, the mask is met. The quantization noise violates the mask at 600 kHz. As stated before, QuadPM is capable of more resolution than is implemented in this IC.

Conclusion

An all-digital, signaling-independent, RF modulator and CMOS PA has been demonstrated. The system delivers power efficiently and shows high linearity. These benefits come at the cost of filtering at the output.

Acknowledgements

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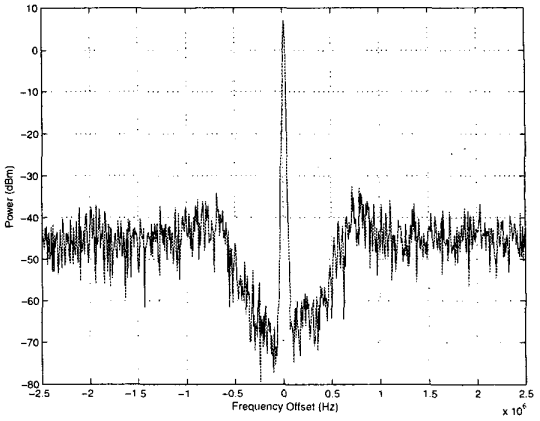

Figure 7: Wide-Band 2-Tone Spectrum

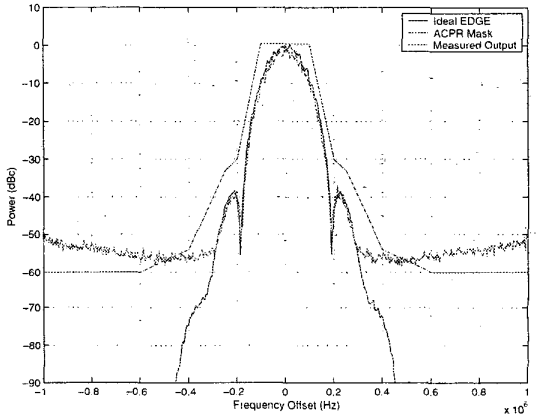

Figure 8: EDGE Spectra and ACPR Mask

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