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High Performance Digital Feedback for PWM Digital Audio Amplifiers

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ABSTRACT

Non-idealities associated with the power stage of pulse width modulated (PWM) based, open loop digital audio amplifiers limit their performance. A high performance digital feedback system corrects for both power supply noise and power stage non-linearity in a PWM digital audio amplifier. An integrated circuit (IC) implementation of this system, along with measured results, is presented. The PWM amplifier, switching between 300 kHz and 400 kHz, achieves an unweighted dynamic range in excess of 100 dB, linearity in excess of 80 dB, and excellent power supply rejection (PSR) with a large scale audio signal.

1. INTRODUCTION

The high power efficiency advantage of switching audio amplifiers has resulted in their widespread use, especially in applications where minimizing size and heat is critical. In such amplifiers, an audio signal which has been pulse modulated is applied to a switching power amplifier which drives a speaker, typically through a passive LC lowpass filter.

Switching amplifiers using pulse width modulation (PWM) have been around for many years [1]. Historically these have been analog based, with the PWM signal generated by comparing a sawtooth waveform to an incoming analog audio signal. By adding some output feedback to the system it is possible to obtain moderate audio quality. Feedback is typically taken from the output of the switches, output of the low pass filter, or a combination of the two.

Switching amplifiers based on pulse density modulation (PDM) have also been implemented [2]. These are typically constructed using a 1-bit sigma delta modulator. By including the switching power stage inside the feedback loop of the modulator, reasonable

rejection of the power stage non-idealities and supply noise can be achieved.

PDM-based amplifiers, however, require a higher switching frequency compared to PWM-based amplifiers, resulting in higher switching losses and lower efficiency. Additionally, with PDM the switching frequency spectrum is audio signal dependent and therefore not well controlled, which can lead to EMI interference issues with adjacent radio tuners. On the other hand, PWM amplifiers have the advantage of both higher efficiency and the ability to tightly control the switching frequency. Furthermore, PWM amplifiers are capable of achieving a higher signal-to-noise ratio (SNR) than PDM amplifiers operating at the same frequency.

PDM modulators and analog PWM modulators ultimately require an analog audio input signal. However, most audio sources today are digital and stored as pulse code modulated (PCM) samples. In recent years, digital PWM amplifiers have been developed [3, 4]. These amplifiers are capable of receiving digital audio PCM input samples and converting them to a digital PWM output signal entirely in the digital domain. Digitally converting from PCM to PWM is implemented using a predistortion algorithm that emulates naturally sampled PWM [5-8]. The PWM edge transitions are quantized in time using a high speed PWM quantization clock. Eight bit quantization is typical, resulting in the need for upsampling and noise shaping in order to produce good in-band noise performance. Very high digital-domain PWM fidelity can be achieved by utilizing a high quality predistortion algorithm [9, 10] and noise shaper [5]. These amplifiers are typically implemented in an open loop configuration.

The performance of digital PWM open loop amplifiers is almost entirely limited by the non-idealities of the power stage and power supply. The switching power stage in a digital amplifier introduces nonlinearity and noise into the switched power output signal. Sources of nonlinearity include the nonlinear 'on' resistance of the switches, error during deadtime or break-before-make (BBM) of the switching stage, and finite rise and fall time of the switching stage output. These nonlinearities not only degrade the total harmonic distortion (THD) performance but also reduce the SNR by mixing the out-of-band quantization noise of the digital PWM driving signal into the audio passband.

The power supply can be an additional source of noise and nonlinearity. Standard PWM open loop power stages provide no power supply rejection. Loading of the digital amplifier, other loads connected to the same power supply, and power supply ripple can produce noise at the power supply to the digital amplifier. The output of a digital amplifier is a direct multiplication of the power supply and the digital PWM signal.

Prior attempts to improve fidelity and power supply rejection of a digital PWM amplifier have proposed incorporating an analog-domain feedback mechanism to correct the distortion introduced by these non-idealities [11] or used an analog delay line to re-time the edges of the PWM waveform [12]. These approaches support a limited range of correction and do not provide large corrections to the duty ratio needed to handle power supply transients found in an automotive environment.

This paper describes a high performance digital feedback method for digitally correcting the power stage non-idealities in a digital PWM switching amplifier.

2. IMPLEMENTATION

An IC has been implemented that incorporates high performance digital feedback in a PWM based digital audio amplifier capable of operating between 300 kHz and 400 kHz. This feedback system corrects for all power stage non-idealities, including distortion due to deadtime, nonlinear on-resistance of the power switches, variations in output rise and fall time, and power supply noise.

The feedback system has been integrated along with a high performance digital PWM modulator. A block diagram of the audio signal processing paths is shown in Figure 1.

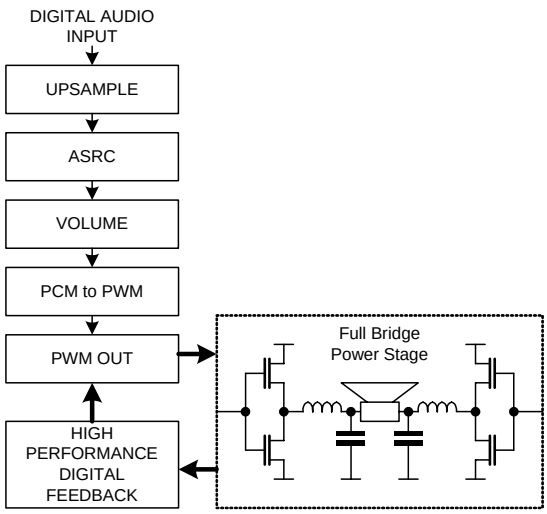

Figure 1 Overall block diagram.

The input PCM signal is upsampled and converted to a rate that is equal to twice the PWM pulse repetition frequency (PRF). An asynchronous sample rate converter (ASRC) is available to accommodate many different input sample rates while maintaining a fixed PWM output rate [13]. A digital volume control function is optimally placed just prior to the PCM-to-PWM conversion block. The PCM-to-PWM conversion block produces an extremely high fidelity digital PWM output signal. This signal is used as a reference signal for the high performance digital feedback block. The high performance digital feedback block generates a digital correction signal that is used to modify the edges of the original PWM signal in order to compensate for power stage non-idealities.

The structure of the high performance digital feedback system is shown in Figure 2. It includes a loop filter, shown in Figure 3, consisting of a cascade of three integrators. The difference between an ideal digital PWM reference signal and a scaled version of the output switching voltage is fed into the first integrator. A combining amplifier provides a weighted sum of the three integrator outputs. The weighted sum is then digitized by a flash analog-to-digital converter (ADC) at a sample rate equal to twice the PRF.

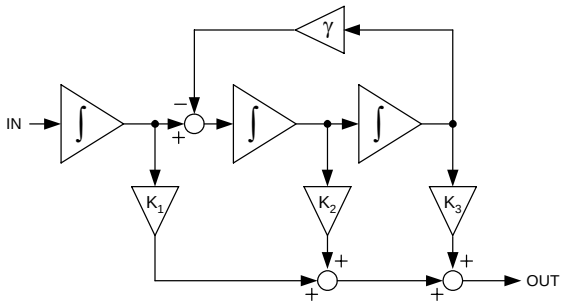

Figure 3 Third order integrating loop filter.

The output of the ADC is used to modify a version of the ideal digital PWM signal to generate a corrected digital PWM signal. The corrected digital PWM signal is amplified by the power stage to create the output switching voltage. Typically, an LC filter is connected between the switching stage and the speaker to suppress the switching frequency and its harmonics.

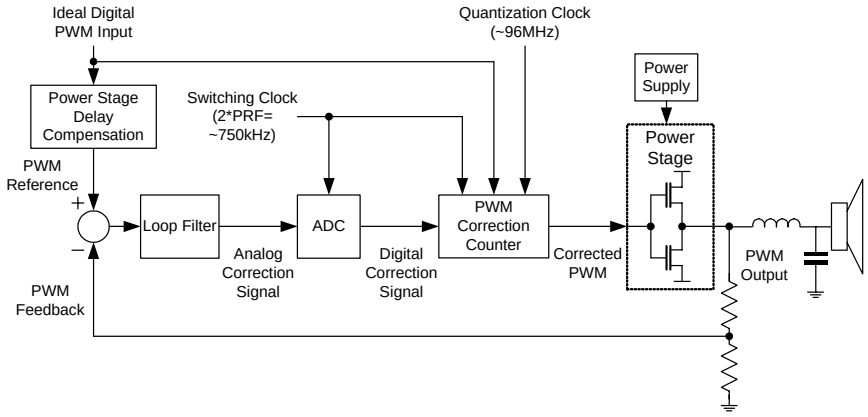

Figure 2 Block diagram of the high performance digital feedback system

The amplitude of the PWM reference signal is determined by an externally applied reference voltage. This reference voltage can be set to a fixed value to achieve a fixed system gain. Alternatively, this reference voltage can be derived from the power stage power supply voltage to allow the feedback system to track DC changes of the power supply.

The pulse edges of the digital PWM signals are defined using a PWM quantization clock. The PWM quantization clock is created using an on-chip PLL locked to a crystal reference. The quantization clock frequency is nominally 96 MHz. The pulse repetition frequency is programmable from 300 kHz to 400 kHz.

This high performance digital feedback system can be described as a sigma delta modulator with a multi-bit quantizer. The noise transfer function (NTF) of the system can be approximated by the following equation [14]:

$$NTF = \frac{1}{1 + \frac{\left(1 - \frac{sT}{4}\right)}{\left(1 + \frac{sT}{4}\right)} \left\{ \frac{k_1}{sT} + \frac{k_2}{\left[(sT)^2 + \gamma\right]} + \frac{k_3}{sT\left[(sT)^2 + \gamma\right]} \right\}} \quad (1)$$

In Equation 1, T corresponds to half of the PWM pulse repetition period, and the γ and k terms correspond to those shown in Figure 3.

At DC the NTF goes to zero. The NTF also goes to zero at a frequency proportional to the square root of gamma (γ). Looking closely at the closed loop output spectra presented in Section 3 below, a shallow spectral null can be observed at approximately 17 kHz that corresponds to the gamma term.

This feedback system has four poles: one pole from each of the three integrators and a fourth pole due to the delay between the ADC output sample and the subsequent PWM edge. As indicated in Figure 2, the feedback loop operates at twice the PRF. Each rising and falling edge of the digital PWM signal is independently modified by the loop.

2.1. Dynamic Range Considerations

There are a number of variables that impact the dynamic range of the high performance digital feedback system. These fall under two key categories: 1) Timing constraints, and 2) Feedback saturation.

2.1.1. Timing Constraints

This IC supports both standard PWM modulation (sometimes referred to as class AD modulation) and suppressed carrier modulation (sometimes referred to as class BD modulation). Standard PWM modulation produces a standard complementary output, and supports both full bridge and half bridge power stage configurations. Suppressed carrier PWM modulation produces a differential PWM output signal for driving a full bridge power stage that results in the differential cancellation of the PWM pulse repetition frequency and its odd harmonics. Suppressed carrier PWM modulation requires a full H-bridge power stage. The high performance digital feedback system is compatible with both standard and suppressed carrier PWM modulation modes. However, as will be explained further, using feedback with suppressed carrier PWM modulation and a full bridge power stage has an advantage of improved dynamic range capability.

The ADC quantizer in the high performance digital feedback loop samples the analog correction signal at a rate equal to twice the pulse repetition frequency. Each ADC output sample is used to correct the subsequent PWM pulse edge. Figure 4 shows the ADC timing for standard PWM modulation with a full H-bridge power stage. Figure 5 shows the ADC timing for suppressed carrier PWM modulation. In these figures, the PWM waveform labeled “Side A Output” corresponds to the PWM signal that drives one side of a full bridge power stage. The PWM waveform labeled “Side B Output” corresponds to the PWM signal that drives the other side of the full bridge power stage. Proper loop stability requires that each PWM edge be corrected by the ADC sampled output captured at the beginning of the corresponding PWM half cycle. This restriction limits the usable dynamic range of the system, since for exceedingly large or small duty ratios the time between the ADC sample capture and the following PWM pulse edge can become too small for proper operation.

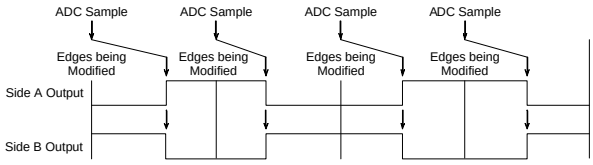

Figure 4 Feedback correction timing for standard PWM modulation

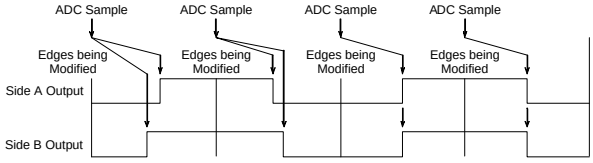

Figure 5 Feedback correction timing for suppressed carrier modulation

The dynamic range limitations associated with ADC sample timing can be circumvented by dynamically shifting the phase of the ADC sample time as a function of the PWM duty ratio [15]. When the duty ratio becomes smaller or larger than predetermined thresholds, the phasing of the ADC sampling is shifted 90 degrees relative to the pulse repetition period. This is illustrated in Figure 6 for a small PWM duty ratio and Figure 7 for a large PWM duty ratio.

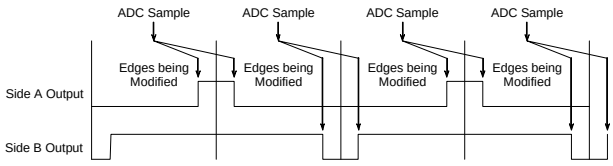

Figure 6 Feedback correction timing for small duty ratios using suppressed carrier modulation. ADC sampling phase shifted 90 degrees.

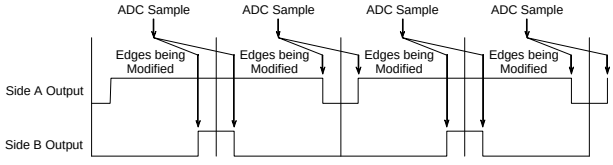

Figure 7 Feedback correction timing for large duty ratios using suppressed carrier modulation. ADC sampling phase shifted 90 degrees.

In the high performance digital feedback system, every PWM edge is modified by the previous ADC sample. The cases illustrated in Figure 4 and Figure 5 show each ADC correction sample modifying one PWM edge per half bridge of the full bridge system. For the cases of either small or large duty ratio as illustrated in Figure 6 and Figure 7, each ADC correction sample will modify both the rising and falling edges of the pulse on one half of the bridge.

To ensure smooth transitions between the ADC sampling phase modes, hysteresis is used. Figure 8 shows the hysteresis plot for transitioning between nominal ADC sampling (Mode B) and phase shifted ADC sampling (Modes A and C).

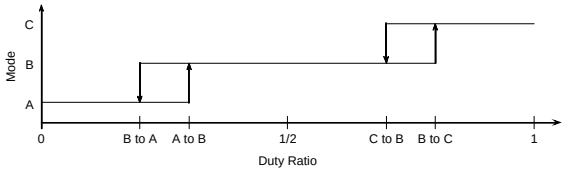

Figure 8 Hysteresis associated with transitions between ADC sampling phase modes. Mode B = nominal ADC sampling. Modes A and C = phase shifted ADC sampling.

2.1.2. Saturation

The duty ratio of a PWM signal is defined as the time the signal is at a logic 'high' divided by the PWM switching period. To obtain the highest possible power output from a power stage it is necessary to be able to saturate to both 0% and 100% duty ratio. For the case of the ideal (unmodified) digital PWM signal being at 0% or 100% duty ratio, no PWM edge modification is possible in one direction. Therefore, error can accumulate in the loop integrators and saturate one or more of them. The high performance digital feedback system is capable of modifying the PWM duty ratio by up to +/- 25% of the pulse repetition period. Very large errors combined with a large audio signal swing can result in modified duty ratios saturating at 0% or 100%. A saturation handling scheme ensures stability during these saturation events. This involves resetting one or more integrators in a controlled manner such that the system poles are stable under all conditions.

The saturation handling capability of the high performance digital feedback system is illustrated in the oscilloscope plots shown in Figure 9 and Figure 10. In these plots, a high amplitude audio input tone is applied

to the power stage. The power stage supply voltage has been reduced from a nominal 14.4 volts to 10 volts while keeping the PWM reference voltage fixed. The high performance digital feedback system compensates for this loss in power stage gain, resulting in feedback loop saturation and clipping of the sinewave peaks. Note the graceful transition into and out of 0% and 100% PWM duty ratio. This saturation behavior is similar to that of a class AB amplifier when the ideal output voltage is beyond the power supply rails.

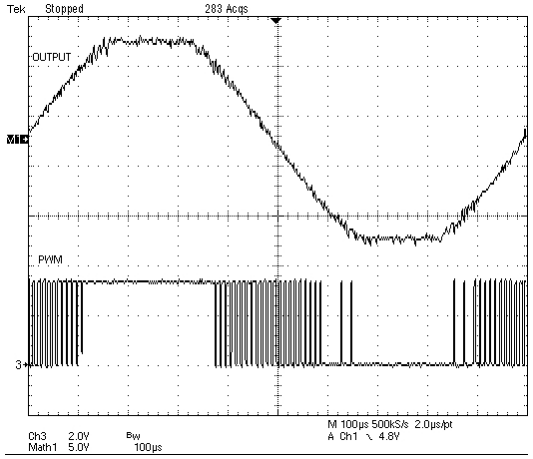

Figure 9 Saturation handling with 1 kHz input audio tone. Differential output voltage across the speaker load (top). PWM driving signal (bottom).

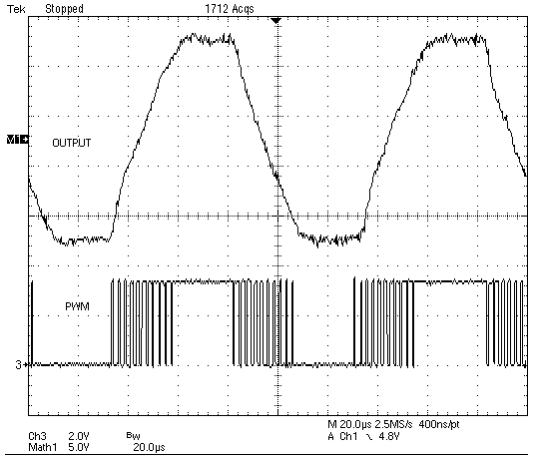

Figure 10 Saturation handling with 10 kHz input audio tone. Differential output voltage across the speaker load (top). PWM driving signal (bottom).

3. PERFORMANCE

Small signal, large signal, and power supply rejection characteristics are presented in this section. All of the results were measured using Freescale Semiconductor's FSA95601 EVM board with discrete H-bridge power stages and suppressed carrier PWM modulation. Spectral measurements utilized Audio Precision AUX25 and AES17 filters.

3.1. Small Signal Behavior

The PWM duty ratio is noise shaped by the high performance digital feedback circuit. When the digital PCM input is set to digital silence the PWM output shows the nature of this noise shaping. In Figure 11 a digital PWM rising transition is shown in the time domain by cycling through thousands of PWM cycles. The digital PWM pulse edge shows five different discrete time placements. The most common is the center time placement corresponding to the case of no correction. This is followed by a correction of plus or minus one quantization clock period. Less frequently, there is a correction of plus or minus two quantization clock periods. Corrections in excess of plus or minus two quantization clock periods are not observed under these conditions. The quantization clock period and corresponding digital PWM edge corrections are in discrete steps of about 10.5 ns.

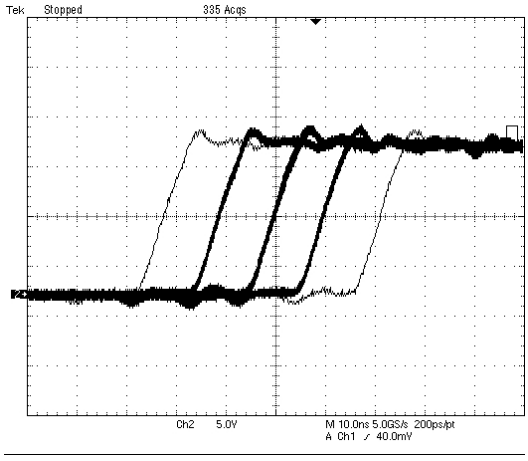

Figure 11 Quantized digital PWM correction edges showing noise shaping of the high performance digital feedback system.

In Figure 12 the spectral output is shown with a minus 60 dB input tone at 1 kHz for an open loop system (high performance digital feedback is disabled). No harmonics of the 1 kHz tone are observed but the noise floor is elevated. By contrast, the spectral output shown in Figure 13 with the same input produces a very different noise floor when the digital feedback loop is enabled. The noise floor is lowered by about 30 dB by the feedback loop under this condition. The unweighted signal to noise ratio relative to 0 dB (normalized to the signal level necessary for achieving 10% THD) is 105 dB measured over the 20 kHz audio band.

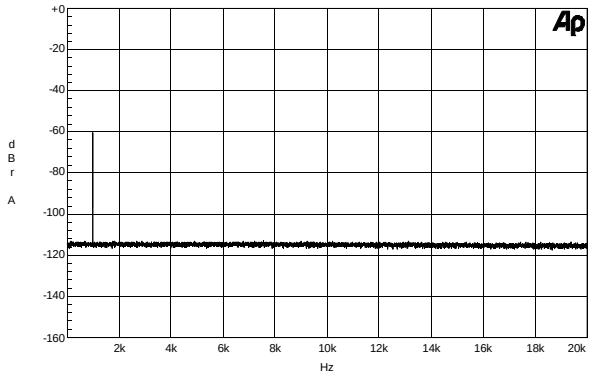

Figure 12 Open loop, -60 dB (relative to 10% THD), 1kHz input tone, 14.4 volt supply, 4 ohm load, PRF = 400 kHz

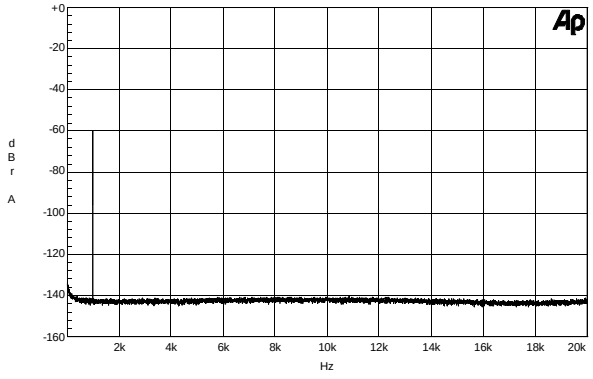

Figure 13 Closed loop, -60 dB (relative to 10% THD), 1kHz input tone, 14.4 volt supply, 4 ohm load, PRF = 400 kHz

3.2. Large Signal Behavior

Under large signal conditions the open loop system displays both harmonic tones of the input signal as well as an elevated noise floor. In Figures 14 and 15 the input is a 1 kHz PCM signal at a level 6 dB below the volume level of signal that would produce 10% THD. Under these conditions the spectrum plots with and without the high performance digital feedback system are shown. The open loop THD is -45 dB (0.56%) whereas the closed loop THD is -93 dB (0.0022%).

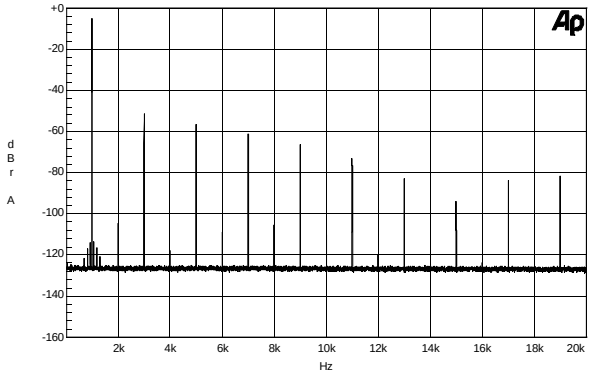

Figure 14 Open loop, -6 dB (relative to 10% THD), 1kHz input tone, 14.4 volt supply, 4 ohm load, PRF = 400 kHz

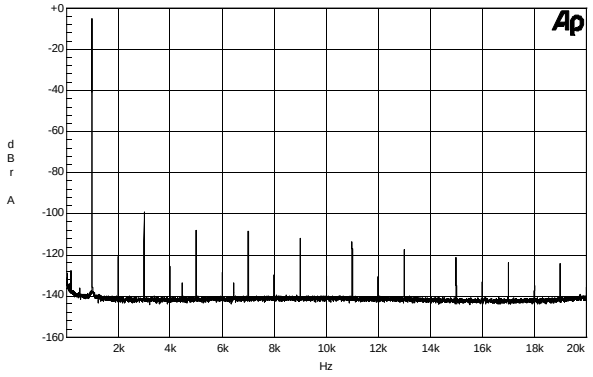

Figure 15 Closed loop, -6 dB (relative to 10% THD), 1kHz input tone, 14.4 volt supply, 4 ohm load, PRF = 400 kHz

Another test of amplifier performance is an intermodulation distortion (IMD) test. This test uses a two tone input signal consisting of 19 kHz and 20 kHz at a -6 dB level. Figure 16 shows the open loop spectrum and Figure 17 shows the closed loop spectrum. The third order IMD term in this case is improved from -45 dB to -80 dB by the action of the high performance digital feedback loop.

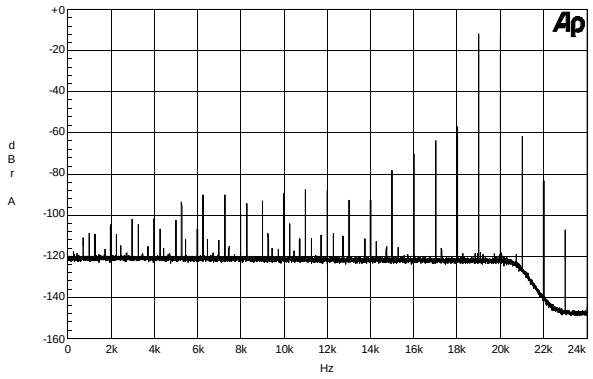

Figure 16 Open loop, -6 dB IMD (relative to 10% THD), 19 kHz and 20 kHz input tones, 14.4 volt supply, 4 ohm load, PRF = 400 kHz

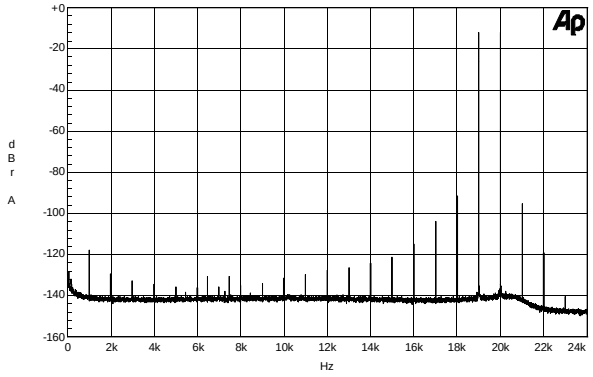

Figure 17 Closed loop, -6 dB IMD (relative to 10% THD), 19 kHz and 20 kHz input tones, 14.4 volt supply, 4 ohm load, PRF = 400 kHz

3.3. Large signal clipping

High performance higher order feedback loops are susceptible to degradation under saturation events. Figure 18 and Figure 19 show the output spectrum under an extreme saturation event. Since the correction required is in excess of the maximum theoretical duty ratios of 0% and 100% there is little improvement in the spectrum by the feedback action. However, no degradation or spurious tones are observed, indicating that the system displays large signal stability during saturation.

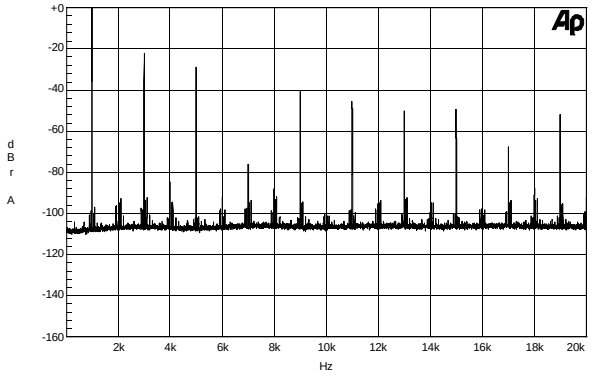

Figure 18 Open loop, 0 dB (relative to 10% THD), 1kHz input tone, 14.4 volt supply, 4 ohm load, PRF = 400 kHz

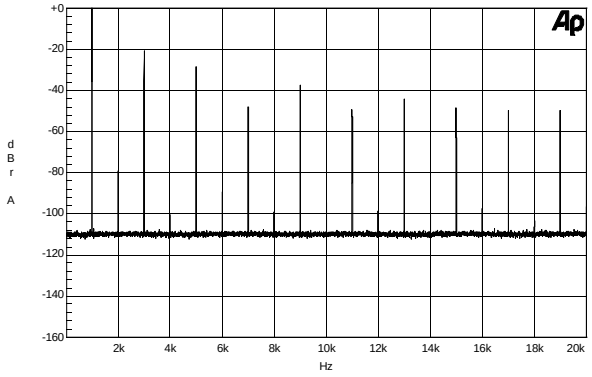

Figure 19 Closed loop, 0 dB (relative to 10% THD), 1 kHz input tone, 14.4 volt supply, 4 ohm load, PRF = 400 kHz

3.4. Power Supply Rejection

Claims of high power supply rejection (PSR) for open loop digital PWM-based audio amplifiers have been made by others [16]. These claims are based on the traditional PSR measurement approach which uses no

audio input signal or tone. However, this approach is not truly valid when considering a switching amplifier. In a PWM switching amplifier, the switched output signal is determined by the product of the switching logic signal and the power supply voltage. For both standard and suppressed carrier modulation and a full bridge configuration the duty ratio on the second side of the bridge is the complement of the duty ratio on the first side of the bridge, and the differential switched voltage, V_{SW}, can be written in terms of the duty ratio, D, and the power supply to the bridge, V_{DD}:

$$Vsw = V_{DD}(2D-1) \qquad (2)$$

When there is no audio signal the duty ratio, D, is fixed at a value of ½. In this case, as shown by Equation 2, perturbations on the power supply, V_{DD}, are mostly zeroed out. This is illustrated in Figure 20 which shows the open loop output spectrum with a fixed 50% PWM output duty ratio (corresponding to a muted audio input signal) and a 1 Vpp 120 Hz filtered square wave added to the power supply. In this case, very little power supply noise is coupled to the output.

Equation (2) is an averaged model of the system. In the suppressed carrier mode the instantaneous voltage across the full bridge is identically zero if the duty ratio is equal to ½. PSR measured under this condition is limited only by the matching of the two sides of the full bridge power stage. Since all nonzero outputs are generated by using the power supply, it is theoretically impossible to have good power supply rejection in completely open loop systems.

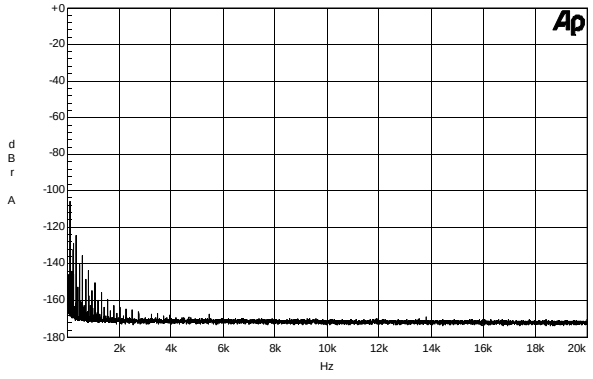

Figure 20 Open loop, PWM muted with 'quiet enable', 14.4 volt supply, 4 ohm load, PRF = 400 kHz, 1 Vpp 120 Hz filtered square wave added to power supply.

Proper PSR evaluation of a switching amplifier requires an audio signal to be present. Measurements made with a large audio input tone allow intermodulation products due to power supply noise to be observed. Figure 21 shows the spectral output with a large (-6 dB) amplitude 1 kHz input tone in the presence of a 1 Vpp 120 Hz filtered square wave added to the power supply. Note the multitude of intermodulation tones centered around both the fundamental 1 kHz tone and its harmonics.

Figure 22 shows the corresponding closed loop response under the same input and power supply conditions. The peak intermodulation tones at 880 Hz and 1120 Hz have been suppressed by the high performance digital feedback system by nearly 60 dB.

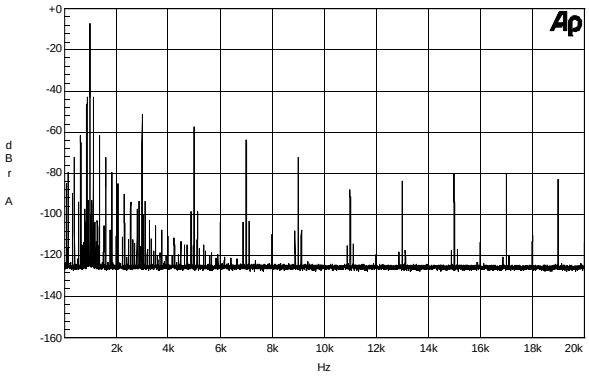

Figure 21 Open loop, -6 dB (relative to 10% THD), 1 kHz input tone, 14.4 volt supply, 4 ohm load, PRF = 400 kHz, 1 Vpp 120 Hz filtered square wave added to power supply.

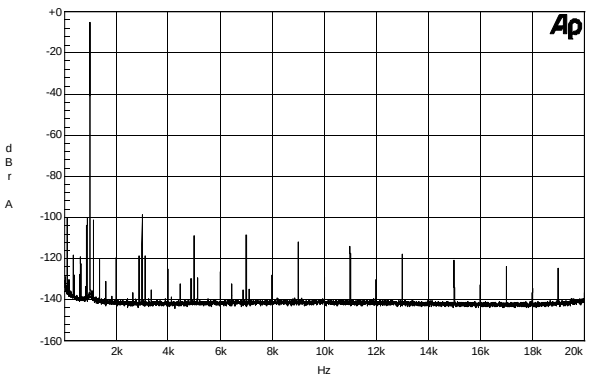

Figure 22 Closed loop, -6 dB (relative to 10% THD), 1 kHz input tone, 14.4 volt supply, 4 ohm load, PRF = 400 kHz, 1 Vpp 120 Hz filtered square wave added to power supply.

3.5. Electromagnetic Interference (EMI) Considerations

Electromagnetic interference (EMI) is a key concern associated with the implementation of switching audio amplifiers. One method to reduce EMI is to slow down the edge transitions at the output of the switching power stage. In an open loop design this results in degraded linearity and noise performance. However, this performance degradation can be compensated and corrected using the high performance digital feedback. The high performance digital feedback system is capable of achieving THD of better than -80 dB (<0.01%) with power stage slew rates as slow as 80 ns. The corresponding dynamic range, measured over the 20 kHz audio bandwidth, is greater than 100 dB.

4. CONCLUSIONS

The technology presented here has been implemented into a six-channel digital audio amplifier controller IC by Freescale Semiconductor, Inc. (part number FSA95601). The integration of the associated analog circuits with the large digital signal processing blocks provides a highly integrated digital amplifier solution. The performance obtained from this IC shows that the high performance digital feedback system is a viable method for correction of power stage nonlinearities and power supply noise. This system is capable of correcting for large signal disturbances, making it suitable for applications that have large power supply transients such as automotive audio systems. This enables the implementation of a cost effective and EMI friendly digital amplifier.

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