

Tracking Power Converter for Supply Modulation of RF Power Amplifiers

Pallab Midya, Ken Haddad, Larry Connell, Steve Bergstedt and Bill Roeckner

IC Design Technology Lab, Motorola Labs, Schaumburg, IL 60196

email: pallab.midya@motorola.com

Abstract - This paper describes a tracking power converter and the controller IC for its implementation. The tracking power converter is used for supply modulation of a linear RF power amplifier. Supply modulation improves RF power amplifier efficiency for variable envelope RF signals. This system maximizes tracking bandwidth (~160kHz), ripple suppression (~70dB) and power conversion efficiency (~92%) with a relatively low switching frequency (800kHz).

I. INTRODUCTION

A majority of dc to dc power converters are designed for applications where the load voltage is fixed and the load impedance varies. Thus, dynamic response is required only to respond to changes in load impedance and input supply. Supply modulation of RF power amplifiers has a different set of requirements. The reference voltage needs to track a moving reference, the load impedance is relatively constant, and rejection of noise in the input supply is necessary.

Due to fast tracking requirements, current mode control was considered as an option. However, the efficiency and signal to noise requirements made it undesirable to sense the current for current mode control [2]. Sensorless current mode control [1], which has similar tracking performance but significantly better SNR performance, was chosen.

II. ENVELOPE FOLLOWING

Envelope Elimination and Restoration (EER) is a well known technique for high efficiency power amplification of variable envelope RF signals [3]. However, the extreme requirements on the individual blocks make it impractical for many applications. Envelope following is a less aggressive technique where the power amplifier supply voltage tracks the envelope of the RF input signal. This system is shown in figure 1. The efficiency performance is close to the maximum efficiency of the linear RF power amplifier.

Actual efficiency achieved is about 50% for a 25kHz QPSK (quadrature phase-shift keying) signal at 20W peak RF

power at 1600MHz, which is far greater than 20% achieved with a simple class AB power amplifier and 33% with a Doherty amplifier under the same conditions.

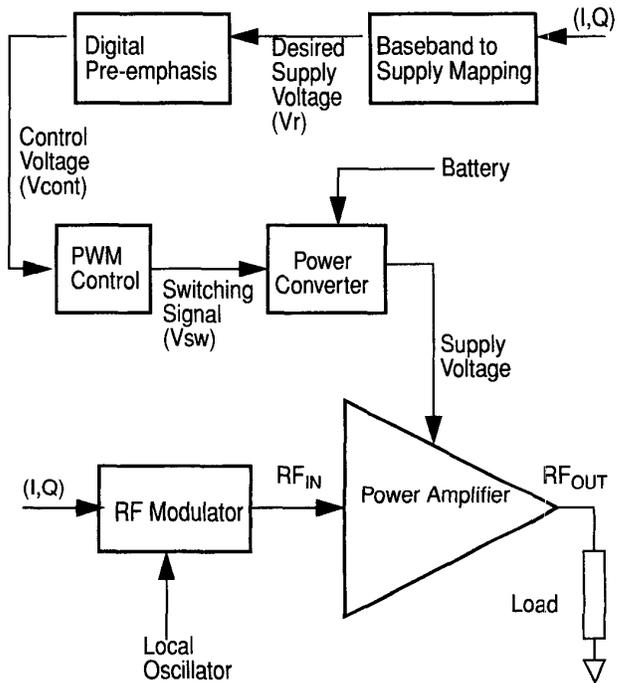


Figure 1: Envelope Following Schematic

Ripple requirements are extremely stringent in supply modulation of RF power amplifiers. The power supply rejection of the RF power amplifier is negligible and an image of the signal occurs at the desired frequency plus or minus the switching frequency. This image needs to be down more than 70dB for many radio applications. In this converter the ripple is suppressed 75dB below the desired signal.

To maintain high power converter efficiency (~90%) the switching frequency has to be kept relatively low. To suppress the ripple sufficiently while passing high frequency signals a higher order output filter is necessary. A four pole L-C filter is

chosen for this application. The control of such a converter poses some interesting challenges. Sensorless current mode control with feedback of the switching signal helps with stability.

In the particular example, the RF channel bandwidth is limited to 25kHz. The bandwidth of the baseband signals (I,Q) is limited to half of that. However, the envelope, being $\sqrt{I^2 + Q^2}$, is not bandlimited. Furthermore, the computation of the squareroot is expensive in terms of signal processing cost. Instead, a bandlimited envelope can be obtained by approximating the squareroot with a polynomial.

$$\sqrt{I^2 + Q^2} \approx a_0 + a_2(I^2 + Q^2) + a_4(I^2 + Q^2)^2 \quad (1)$$

The coefficients are optimized to provide the closest approximation for a given signal distribution. Even though the signal being transmitted is not known in advance the statistical distribution of the signal is known and can be used to compute the coefficients in advance. Reference [4] provides the detailed algorithm for computation of the coefficients. Figure 2 shows an example squareroot approximation. The minimum supply to the RF amplifier was about 1V to avoid phase distortion. The polynomial coefficients were chosen to enforce this condition.

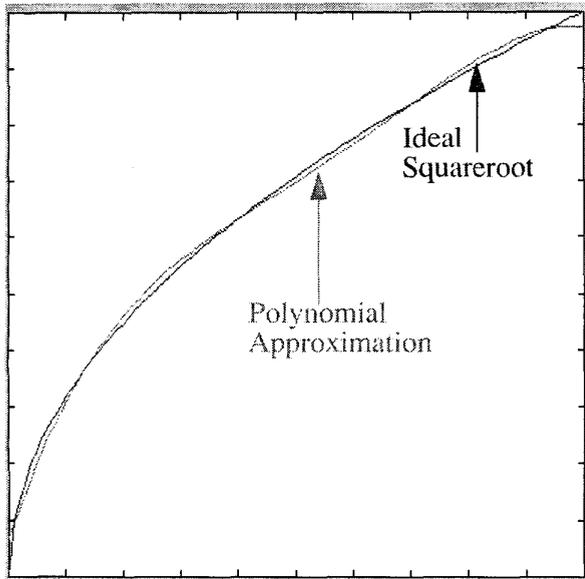


Figure 2: Polynomial Approximation of Squareroot

III. CONTROL SCHEME

This power converter system is particularly sensitive to noise since any noise spur modulates with the RF carrier to create an RF spur close to the carrier frequency. Integral feedback based on voltages was chosen to suppress most of the noise in the system. This also allowed complete integration of the feedback network, resulting in a compact design suitable for the satellite subscriber handset.

Figure 3 shows the filter and the state variables. Initially, the LC filter was chosen to be a critically damped Legendre filter. The reference at the output V_r can be passed through the inverse of the filter response to get an effective feedforward reference voltage V_{ff} . This is computed using digital signal processing. The switching voltage V_{sw} can be made to track the V_{ff} reference by using appropriate feedback.

$$Sig \propto \int (V_{ff} - V_{sw}) dt \quad (2)$$

Output feedback was found to be necessary for the RF power amplifier being used. To accommodate this the signal Sig was modified as follows.

$$Sig \propto \int [(V_r - V_{out}) + (V_{ff} - V_{sw})] dt \quad (3)$$

The input signal V_{cont} , as shown in figure 4, is chosen to be the average of the reference V_r and the feedforward reference V_{ff} . In effect, it provides pre emphasis to the higher frequencies. This extends the small signal bandwidth to 160kHz.

$$Sig = \int \frac{((V_{cont} - V_{sw}) + (V_{cont} - V_{out}))}{V_{nom} T_s} dt \quad (4)$$

The gain of the feedback signal is chosen based on equal slope criteria of sensorless current mode control and best noise performance [1-2]. Since the reference voltage is variable we can meet the equal slope criteria at only one reference voltage. This is chosen to be V_{nom} in equation 4.

The system response is modified by the addition of the output filter. The output filter component values were transposed to maintain the critically damped nature of the original filter. Filter components L_1 and C_1 are transposed as follows while C_2 and L_2 remain unchanged. Detailed derivation of this is provided in reference [5].

$$L_1' = 2L_1 + L_2 \quad \text{and} \quad C_1' = \frac{2C_1 L_1}{2L_1 + L_2} \quad (5)$$

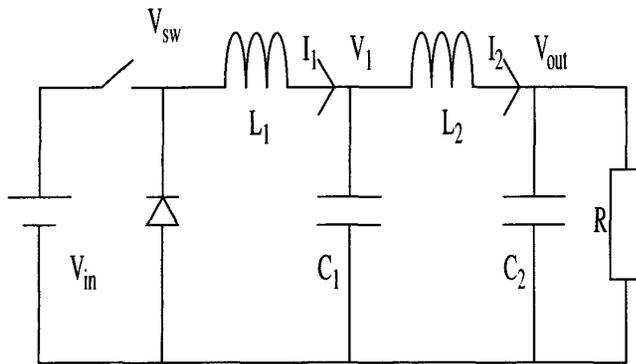


Figure 3: Buck Converter Schematic

IV. IC IMPLEMENTATION

Integrated feedback is implemented in the error amplifier using an opamp and RC components as shown in figure 4. Synchronization to the main system clock of the radio is critical for robust operation. Unlike hysteresis based control which results in a variable switching frequency this system has a fixed switching frequency based on a clock pulse sent from the radio.

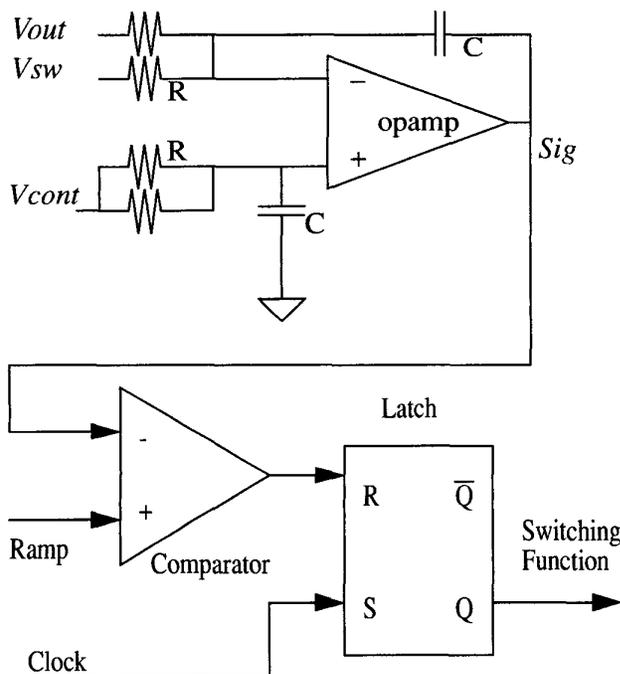


Figure 4: Controller Structure

The ramp generator is implemented as a resettable integrator and is laid out with similar RC elements as the error amplifier. The opamps for both the error amplifier and ramp generator are identical and laid out adjacent to each other on the IC. Thus, noise from the substrate and power supply couples in a similar manner to both, minimizing the effect of this noise at the output of the comparator. Further isolation techniques, such as guard rings, were implemented to minimize coupling of switching noise into these analog circuits.

The variation of the RC product when implemented with on chip resistors and capacitors is +/-40%. However, the gain of the ramp and the feedback structure track almost exactly, resulting in cancellation of the variation.

The power MOSFETs are external but the gate drive is integrated. The gate drive supports a synchronous rectifier drive for high efficiency. The gate drive current is about 1A. The gate drive structure was optimized for charging and discharging the gate charge in less than 10ns. To limit shoot through current in the IC as well as the gate drive, the gate drive was constructed as a combination of parallel stages that were turned on in sequence.

The self and mutual inductance in the bond wire, lead frame and PCB was modelled and included in SPICE simulation of the IC. The pin placements were chosen to minimize self inductance. Voltage spikes at switch transitions were further minimized by the mutual inductance.

For example, the output gate drive pin is sandwiched between the power ground and power Vdd pins. To further reduce inductance some pins and bond wires are doubled up as well. The effective loop inductance has been brought down to less than 0.5nH.

The IC was designed for a specified switching frequency of 800kHz and a particular LC filter. However, the design is general enough to operate at up to twice the switching frequency and an arbitrary filter impedance and corner frequency.

V. SIMULATION AND EXPERIMENTAL RESULTS

Tracking with the RF envelope was simulated. The pre emphasis of high frequencies and delay compensation was included in the reference. Figure 5 shows a tracking simula-

tion where the reference and envelope sit right on top of each other and are almost indistinguishable except at a signal null.

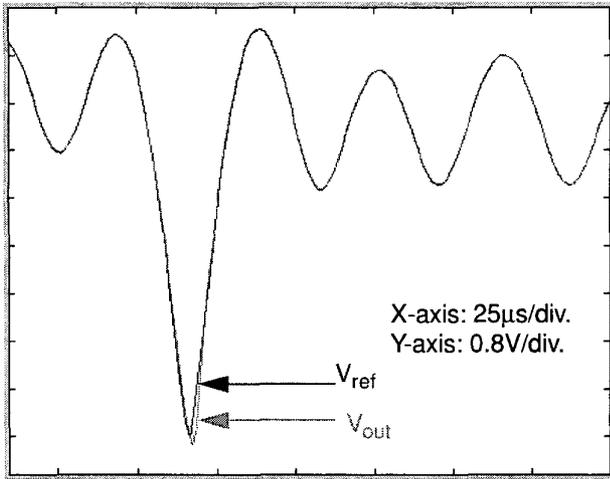


Figure 5: Tracking Simulation

Measured envelope tracking response was excellent and matched simulations very closely as shown in figure 6. Delay compensation of the reference was not performed, and we see about 2µs of delay through the converter system. By contrast, in figure 5 the delay was compensated by advancing the reference.

Linearity is measured by putting a single tone in the reference and looking at second and third harmonics. The linearity is very good at low frequencies and degrades at higher frequencies. However the higher amplitudes occur at low frequencies. Figure 7 shows a plot of the second and third harmonics.

External parts required are minimal. The complementary power MOSFETs fit in a single package. To bias the circuit a single bias resistor is necessary. The remaining external parts are the inductors and bypass capacitors. Figure 9 shows the circuit diagram of the controller IC and external parts.

Peak efficiency of the power converter exceeded 90%. Average efficiency when tracking the RF envelope was approximately 90%. Figure 8 shows the efficiency as a function of power.

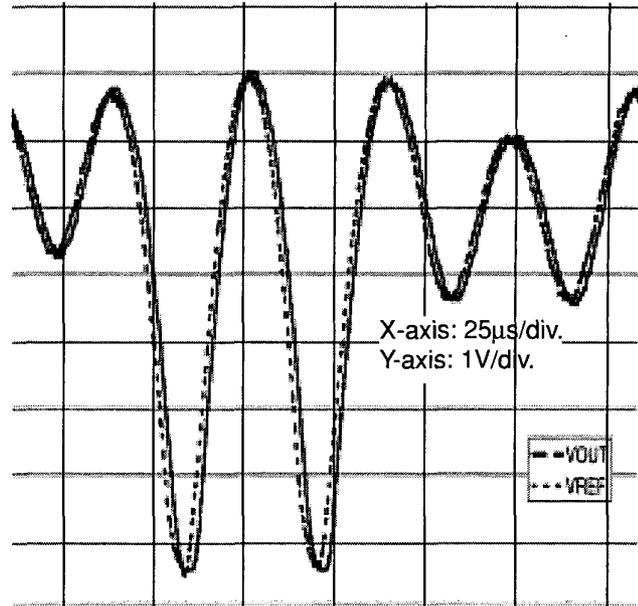


Figure 6: Envelope Tracking

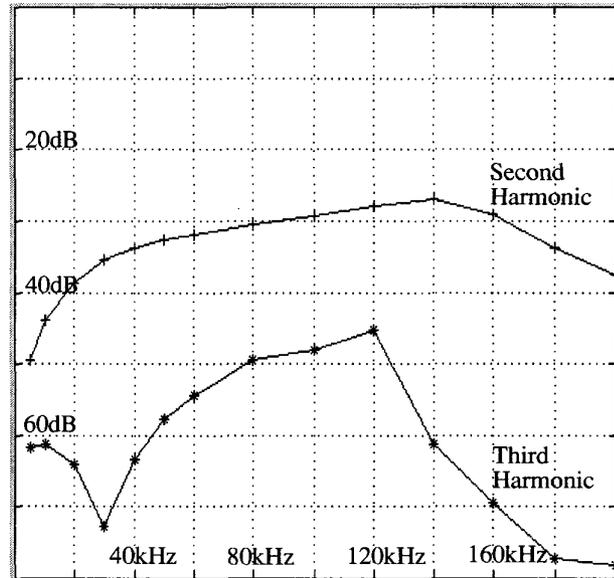


Figure 7: Harmonic Distortion

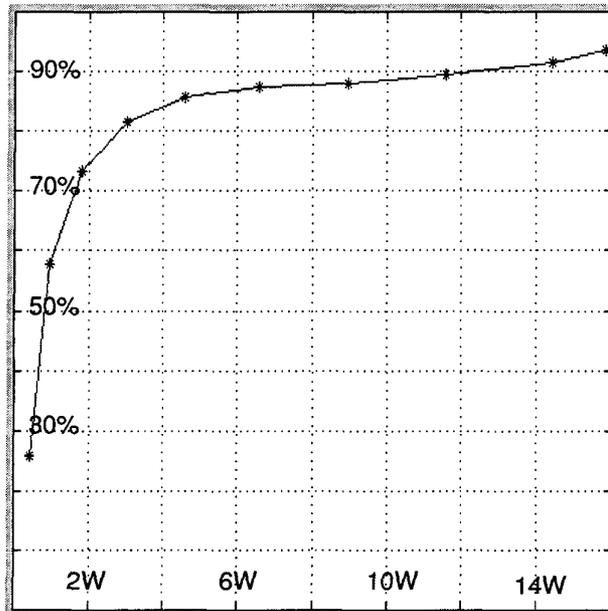


Figure 8: Efficiency of Converter

The controller IC was used in a satellite phone to provide a system solution for power savings in an RF power amplification system. Apart from increasing efficiency, this also resulted in a cost reduction because a less costly RF power amplifier could be used. The control function was fully integrated. The RF power amplifier with the tracking power supply was tested and met all regulatory requirements for linearity and out of band emissions.

VI. SYSTEM SPECIFICATIONS

Input Voltage: 8V to 14V
 Output Voltage Tracking Range: 1V to 7V
 Switching Frequency: 800kHz (nominal)
 Converter Efficiency: 90% (nominal)
 Small Signal Bandwidth: 160kHz
 Ripple: <-70dBc
 Delay: 2 μ s (nominal)

VI. CONCLUSIONS

This paper describes a tracking power converter and a controller IC for it. The tracking speed is maximized by using sensorless current mode control and pre emphasis of the reference waveform. The tracking converter is used to implement

supply modulation of an RF power amplifier. Goals of high efficiency, low ripple, and good tracking were achieved. The RF amplifier with supply modulation met all spectrum requirements while having power conversion efficiency of 50% for a QPSK signal.

ACKNOWLEDGEMENTS

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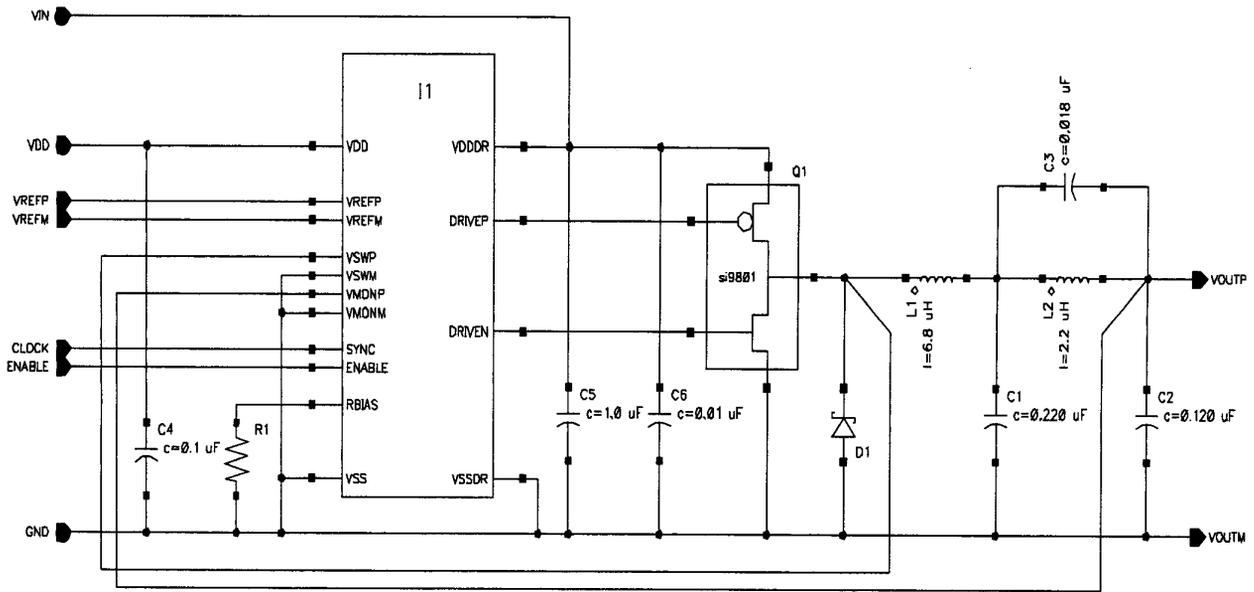


Figure 9: Circuit Diagram of Controller IC and External Parts

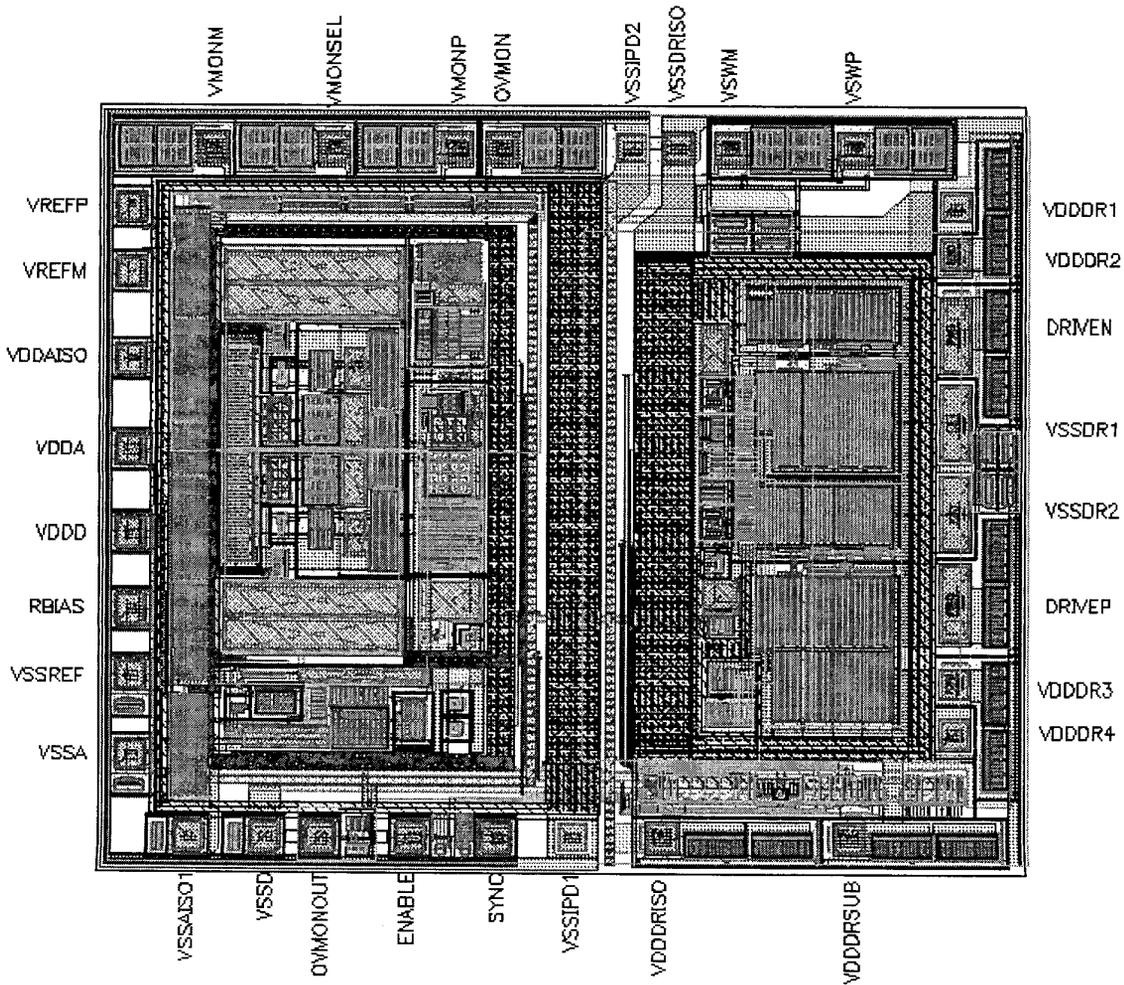


Figure 10: IC Die Plot